

Compal Confidential

TGL-H MB Schematic Document

LA-K455P

Rev: 1.0

2021.05.25

@ : Un-pop Component
@EMI@/@ESD@/@RF@ : EMI, ESD, RF Un-POP Component
EMI@/ESD@/RF@ : EMI, ESD, RF Component
JUMP@/JP@/PJ@ : JUMP
5VFAN@/12VFAN@ : JUMP for FAN power
XDP@ : XDP Component
CONN@ : Connector Component
SW@ : Debug PWR Button
CNV@/@CNV@ : CNVi Support
G3@ : EC G3 Flash Sharing
N18P@/GN20P@ : GPU Support
GN20P0@/GN20P1@/GN20P0D@ : P0/P1/P0-D SKU
VS8GR3@/VM8GR3@/VH8GR1@ : VRAM SKU
VS@/VM@/VH@ : VRAM Support
BBY@ : BBY Support

04/13 PVT change PCB to R3 part



PCB 3K5 LA-K455P REV1 MB GN20P GOLD A31
DAA000ON011
PCB_R3G@



PCB 3K5 LA-K455P REV1 MB GN20P TRIP A31
DAA000ON012
PCB_R3T@

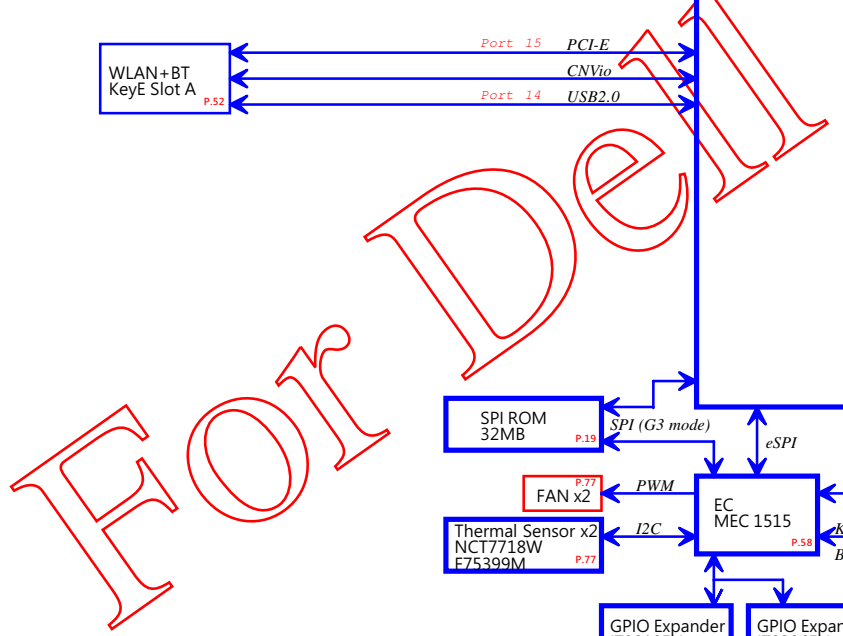


PCB 3K5 LA-K455P REV1 MB GN20P HANN A31
DAA000ON013
PCB_R3H@



PCB 36L LA-K455P REV0 M/B GN20P S
DAA000ON000
PCB@

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Issued Date	2020/03/05	Deciphered Date	2021/12/31	Title	Cover Sheet
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Security Classification		Compal Secret Data		Title	
Issued Date	2020/03/05	Deciphered Date	2018/02/05	Compal Electronics, Inc. Block Diagram	
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Board ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100K	10K	3.000	Pre-EVT
2	100K	17.8K	2.801	EVT
3	100K	27K	2.598	DVT1
4	100K	37.4K	2.402	DVT2
5	100K	49.9K	2.201	Pilot
6	100K	64.9K	2.001	
7	100K	82.5K	1.808	
8	100K	107K	1.594	
9	100K	154K	1.299	
10	100K	200K	1.1	

Power State

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Port	Power Rail	Device	Address
PCH_SMBCLK PCH_SMBDATA	+3VALW_PCH	JDIMM1	0xAA
		JDIMM2	0xA4
PCH_SML1CLK PCH_SML1DATA	+1.8V_PRIM	CCG6SF	0x20

TGL-H-PCH H510

HSIO	USB3.2	PCIe	SATA3	Function
0	1			JUSB1
1	2			
2	3			JUSB (DB)
3	4			JUSB (DB)
4	5			
5	6			
6	7			
7	8			
8				
9				
10				
11				
12				
13				
14		9		
15		10		JSSD2, 2280 SATA x2 / PCIe x4
16		11	0A	
17		12	1A	
18		13	0B	
19		14	1B	LAN
20		15		WLAN
21		16		
22		17		
23		18		
24		19		
25		20		
26		21		
27		22		
28		23		
29		24		

Symbol Note :



Digital Ground

Analog Ground

60 mils/1A = 1/3 oz
40 mils/1A = 0.5 oz
20 mils/1A = 1 oz
10 mils/1A = 2 oz

TGL-H-CPU

PCIe4	Function
0	
1	JSSD1, 2280 PCIe x4 (GEN4)
2	
3	
PCIe16	Function
0	
1	
2	
3	
4	DGPU PEG
5	
6	
7	
TCP0	Function
0	
1	CPU side Type C

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address
GPU_THM_SMBCLK GPU_THM_SMBDAT	+3VS	Thermal 1	0x98h
		Thermal 2	0x9Ah
PBAT_CHG_SMBCLK PBAT_CHG_SMBDAT	+3VALW_EC	GPU (GN20P)	0x9E
		BATTERY	0x16
		CHGR	0x12
DAT_TP_SIO12C_CLK CLK_TP_SIO12C_DAT	+TP_VDD	Touch Pad	0x2C
UPD1_SMBCLK UPD1_SMBDAT	+3V_VSYS	CCG6SF	0x08
		MCU	0xC2
		IO Expander	0x40

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
+12.6V_BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCCIN	CPU FIVR input power supply	ON	OFF	OFF	OFF	OFF
+VCCIN_AUX	PCH FIVR input power supply	ON	OFF	OFF	OFF	OFF
+VCCIN_AUX_PCH	PCH power supply	ON	OFF	OFF	OFF	OFF
+3.3V_BAT_LDO	RTC power	ON	ON	ON	ON	ON
+RTC_CELL	+3.3V_BAT_LDO/+3VLP for suspend power	ON	ON	ON	ON	ON
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW_PCH	+3VALW Primary Power Well for PCH	ON	ON	ON	ON*	OFF
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+1.8V_PRIM	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.05VO_OUT_FET	System +1.05V power rail	ON	ON	ON	ON*	OFF
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+2.5V_MEM	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF	OFF
+1.05V_VCCSTG	Gated version of VCCST	ON	OFF	OFF	OFF	OFF
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+1.8V_RUN	System +1.8VS power rail	ON	ON	OFF	OFF	OFF

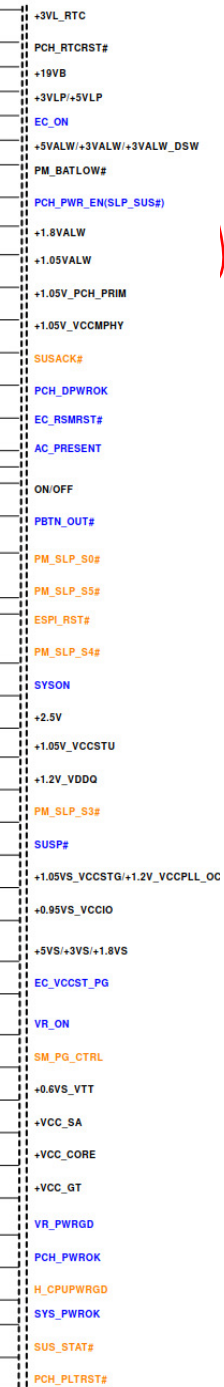
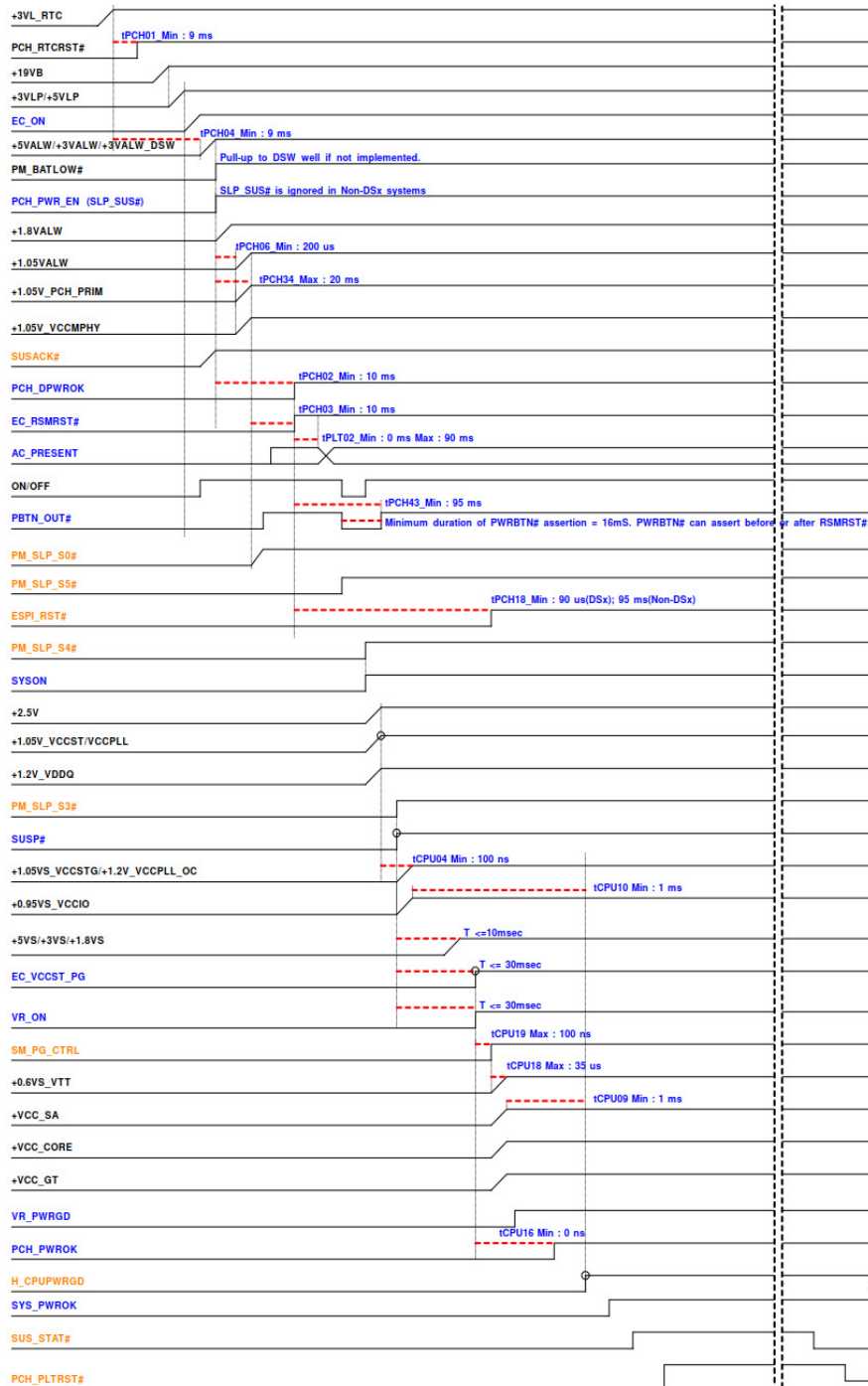
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

G3->S0

S0->S3

S3 ->S0

S0->S5



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2020/03/05		2021/12/31		Power Sequence	
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04/13 PVT change CPU to R3 part

UC1 CPU_I5_11260@

S IC FH8069004351513 SRKT0 R0 2.6G A31 !
SA0000EDEF2L

UC1 CPU_I5_11400@

S IC FH8069004351613 SRKT1 R0 2.7G A31 !
SA0000EEDJ2L

UC1 CPU_I7@

S IC FH8069004352018 SRKT3 R0 2.3G A31 !
SA0000EDK2L



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2020/03/05		2021/12/31		Title	
2021/12/31		TGL-H(1/8)DDI/CSI/Memory		Size	
TGL-H(1/8)DDI/CSI/Memory		Document Number		Rev	
LA-K455P		1.0		Date:	
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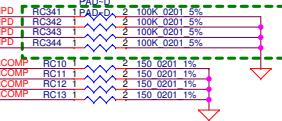
Type-C



NOTE

If the display connector is on the docking station, the hot-plug circuitry should remain on main motherboard and not on the docking station in order to prevent display detection failures related to hot-plug and S-state resume. HPD signal should not be allowed to float anytime.

Follow PDG note

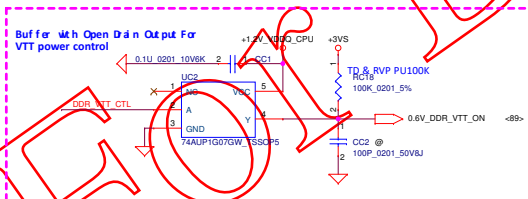
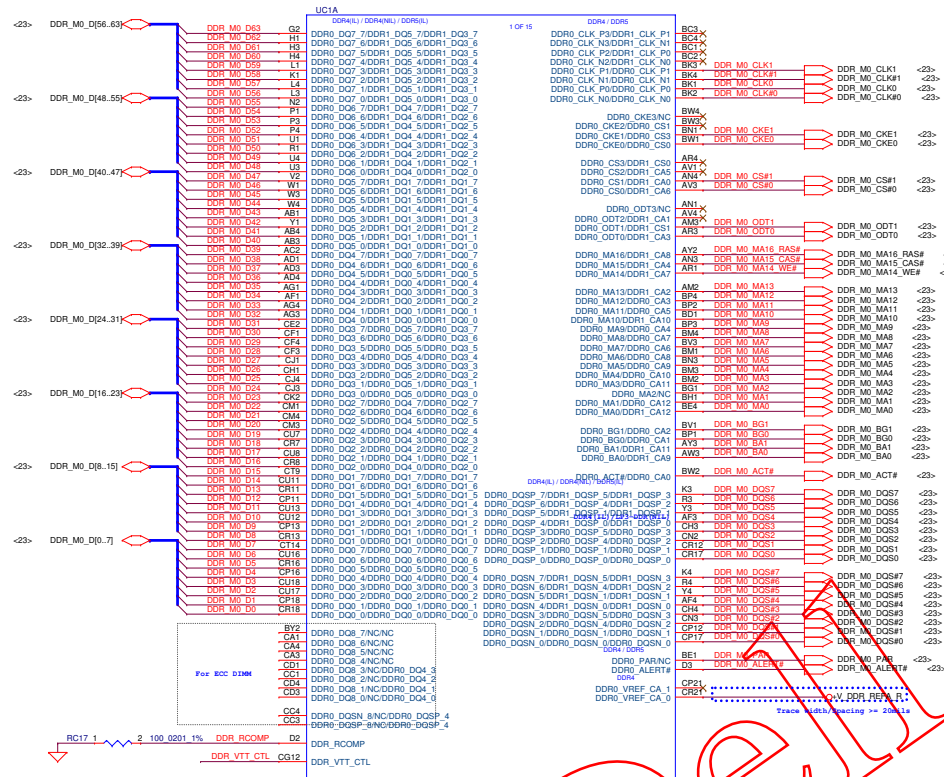


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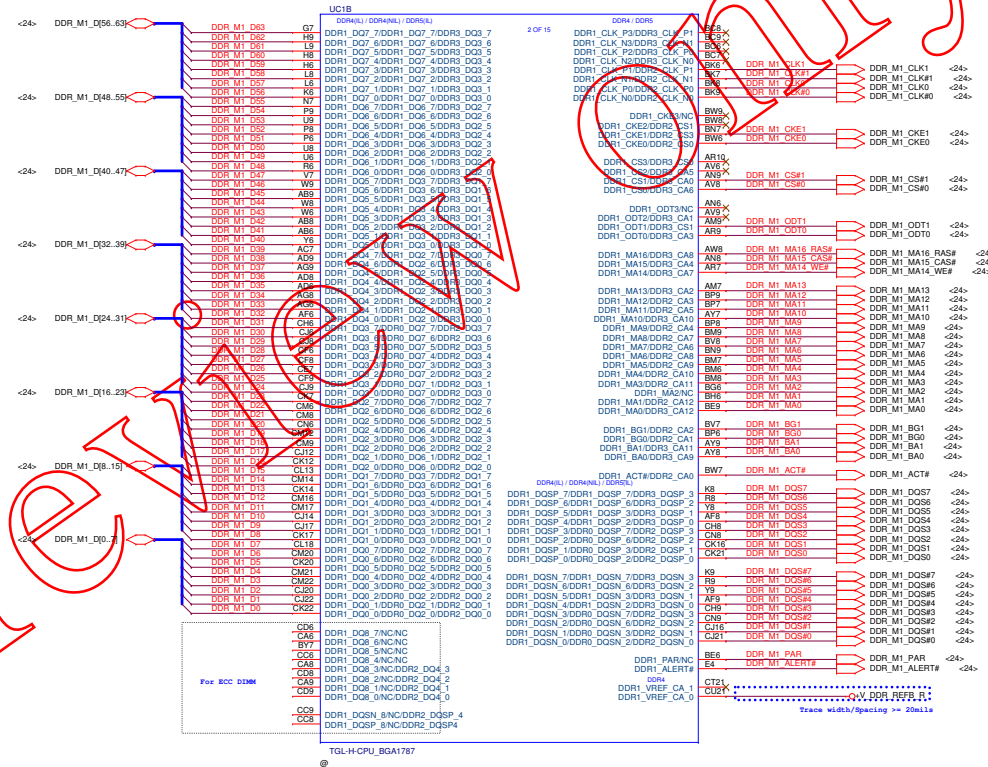
CHANNEL-A

Interleaved Memory



CHANNEL-B

Interleaved Memory



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JSSD1 (GEN 4)

JSSD1 (GEN 4)

To DGPU

SWAP for Layout smoothly

To DGPU

To PCH

To PCH

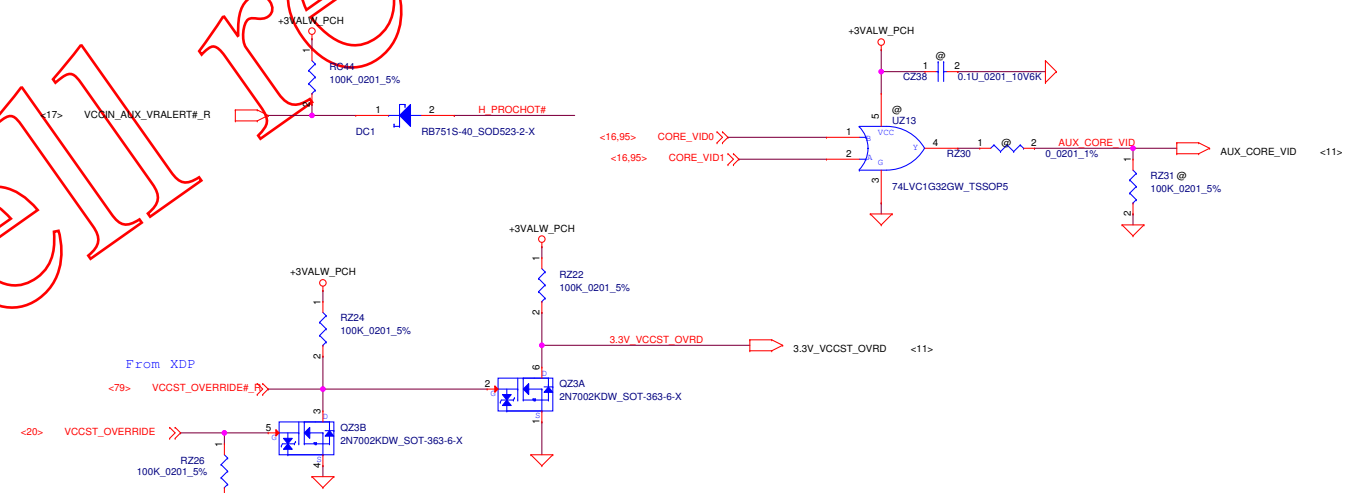
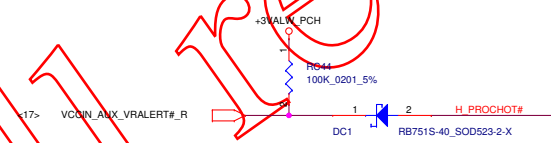
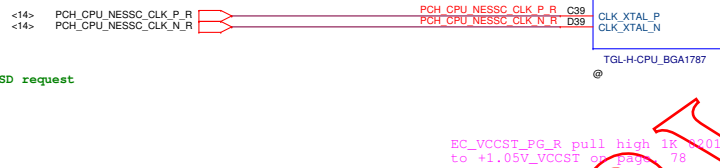
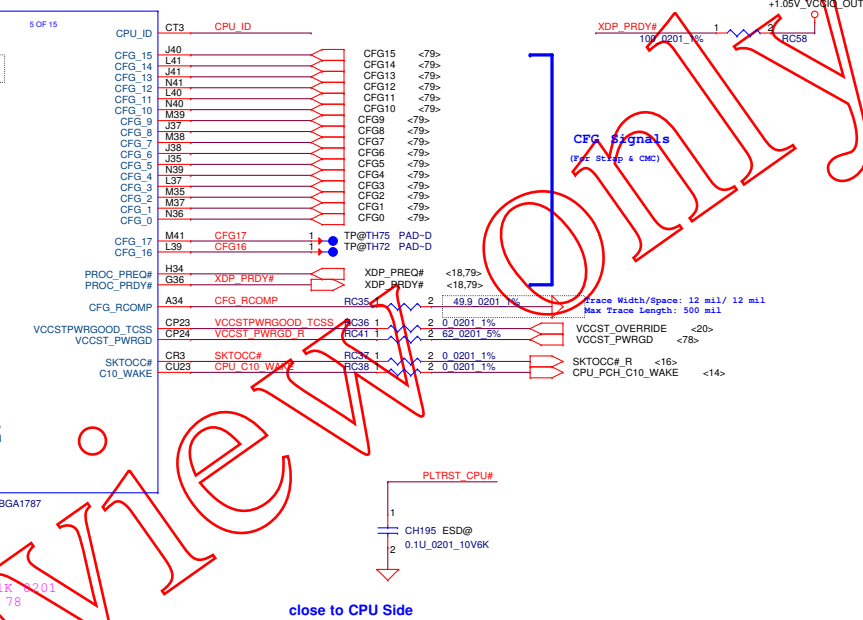
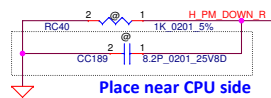
UC1C

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TGL-H-CPU_BGA1787

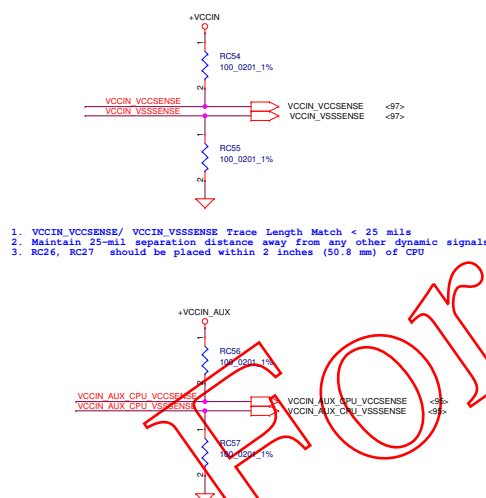
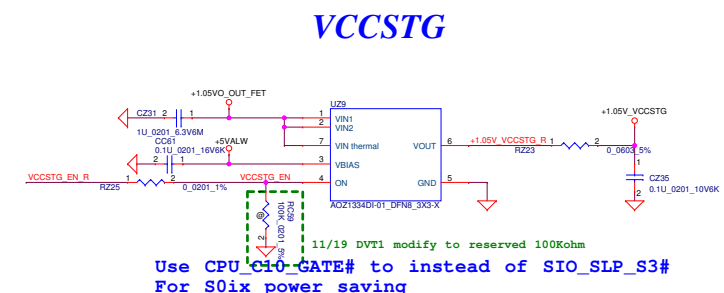
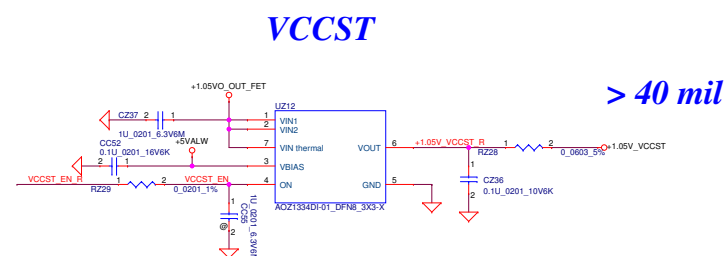
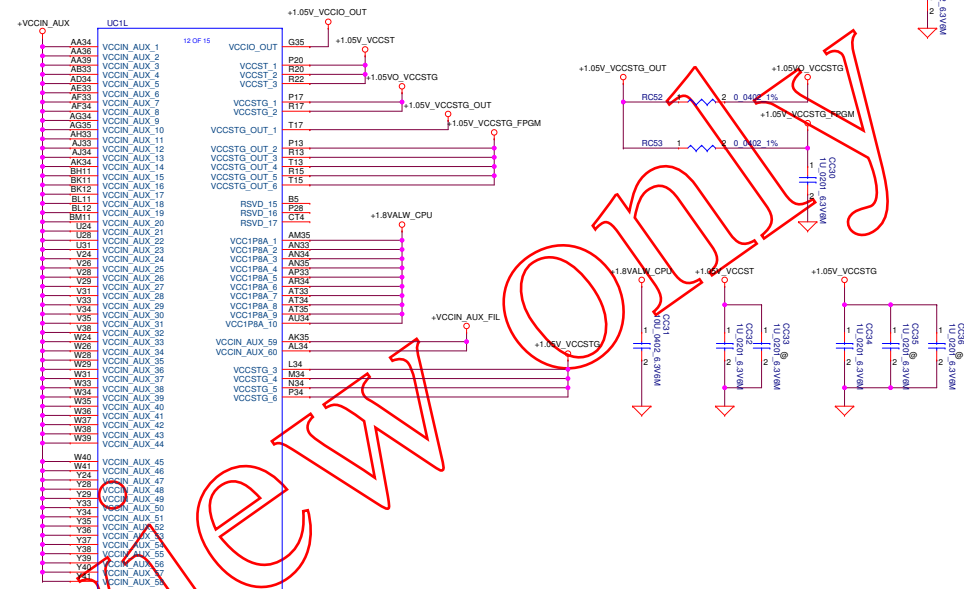
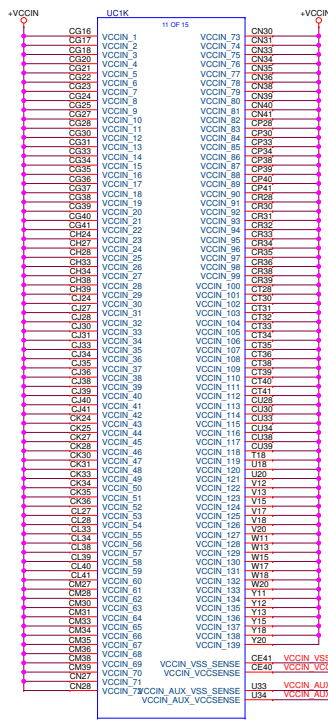
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Layout trace need to avoid PWR

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1. VCCIN_AUX_VSSSENSE / VCCIN_AUX_VCCSENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals
3. RC28, RC29 should be placed within 2 inches (50.8 mm) of CPU

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UC1N

+1.2V_VDDQ_CPU

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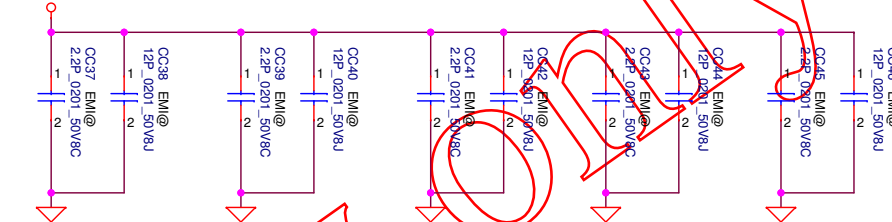
L15 VSS_572 VDD2_1
L18 VSS_573 VDD2_2
L22 VSS_574 VDD2_3
L26 VSS_575 VDD2_4
L29 VSS_576 VDD2_5
L33 VSS_577 VDD2_6
L35 VSS_578 VDD2_7
L36 VSS_579 VDD2_8
L38 VSS_580 VDD2_9
L5 VSS_581 VDD2_10
L7 VSS_582 VDD2_11
M33 VSS_583 VDD2_12
M36 VSS_584 VDD2_13
M40 VSS_585 VDD2_14
N1 VSS_586 VDD2_15
N10 VSS_587 VDD2_16
N13 VSS_588 VDD2_17
N17 VSS_589 VDD2_18
N20 VSS_590 VDD2_19
N24 VSS_591 VDD2_20
N28 VSS_592 VDD2_21
N3 VSS_593 VDD2_22
N31 VSS_594 VDD2_23
N33 VSS_595 VDD2_24
N35 VSS_596 VDD2_25
N37 VSS_597 VDD2_26
N38 VSS_598 VDD2_27
N4 VSS_599 VDD2_28
N5 VSS_600 VDD2_29
N6 VSS_601 VDD2_30
N8 VSS_602 VDD2_31
N9 VSS_603 VDD2_32
P10 VSS_604 VDD2_33
P11 VSS_605 VDD2_34
P15 VSS_606 VDD2_35
P18 VSS_607 VDD2_36
P2 VSS_608 VDD2_37
P22 VSS_609 VDD2_38
P26 VSS_610 VDD2_39
P29 VSS_611 VDD2_40
P33 VSS_612 VDD2_41
P35 VSS_613 VDD2_42
P38 VSS_614 VDD2_43
P41 VSS_615 VDD2_44
P5 VSS_616 VDD2_45
P7 VSS_617 VDD2_46
R10 VSS_618 VSS_652
R18 VSS_619 VSS_653
R2 VSS_620 VSS_654
R33 VSS_621 VSS_655
R34 VSS_622 VSS_656
R36 VSS_623 VSS_657
R39 VSS_624 VSS_658
R5 VSS_625 VSS_659
R7 VSS_626 VSS_660
T20 VSS_627 VSS_661
T22 VSS_628 VSS_662
T24 VSS_629 VSS_663
T28 VSS_630 VSS_664
T31 VSS_631 VSS_665
U10 VSS_632 VSS_666
U13 VSS_633 VSS_667
U15 VSS_634 VSS_668
U17 VSS_635 VSS_669
U2 VSS_636 VSS_670
U22 VSS_637 VSS_671
U26 VSS_638 VSS_672
U29 VSS_639 VSS_673
U35 VSS_640 VSS_673
U38 VSS_641 VSS_673
U41 VSS_642 VSS_673
U5 VSS_643 VSS_673
U7 VSS_644 VSS_673
V1 VSS_645 VSS_673
V10 VSS_646 VSS_673
V11 VSS_647 VSS_673
V22 VSS_648 VSS_673
V3 VSS_649 VSS_673
V36 VSS_650 VSS_673
V51 VSS_651 VSS_673

TGL-H-CPU_BGA1787

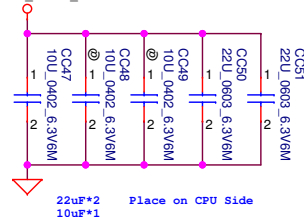
@

EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 5 (EMI@)
2.2pF* 5 (EMI@)

+1.2V_VDDQ_CPU



+1.2V_VDDQ_CPU



Place on CPU Side

+1.8V_PRIM

+1.8V_PRIM_R



+1.8V_PRIM_R

+5VALW

0.1u_0201_10V6K

1 2

CC85

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

<11,16>

CPU_C10_GATE#

RC87

1 2

0 0201 1%

1.8VALW CPU EN

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

I (Max) : 0.5 A(+1.8VALW_CPU)
RON(Max) : 3.5 mohm
V drop : 0.00175 V
Delay time : >10 us & <65 us

UC6

VIN1

VIN2

VIN thermal

VBIAS

ON

GND

AOZ1334DI-01_DFN8_3X3-X

6

VOUT

1

2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

1 2

0.1u_0201_10V6K

Security Classification

Compal Secret Data

Issued Date

2020/03/05

Deciphered Date

2021/12/31

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Compal Electronics, Inc.

Title

TGL-H(7/8)Power VDDQ

Size

Document Number

LA-K455P

Date:

Tuesday, April 20, 2021

Sheet

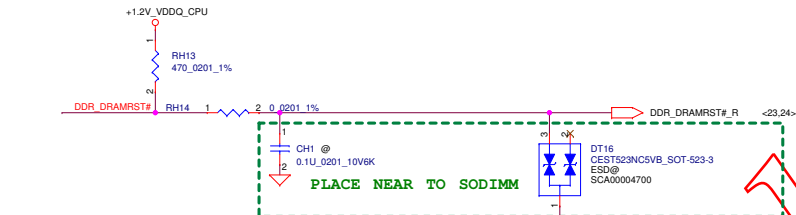
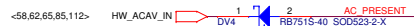
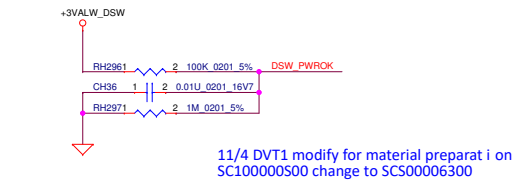
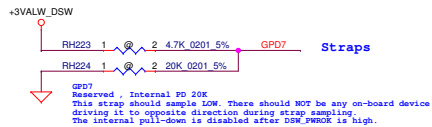
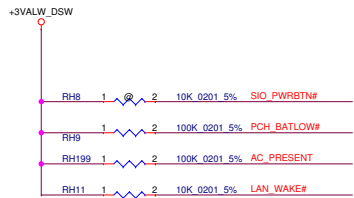
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of

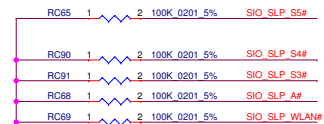
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Rev

1.0

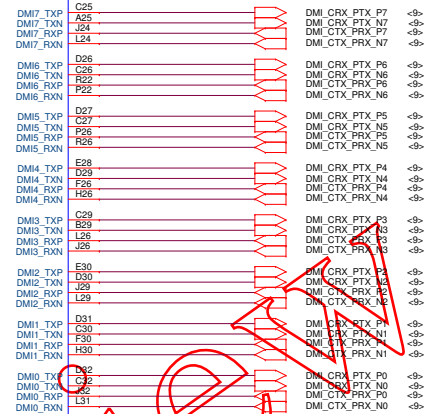
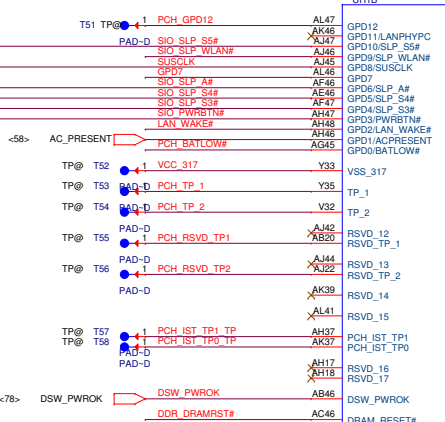


PCH GLITCH ISSUE MITIGATION(PDG 0.7 p.141)

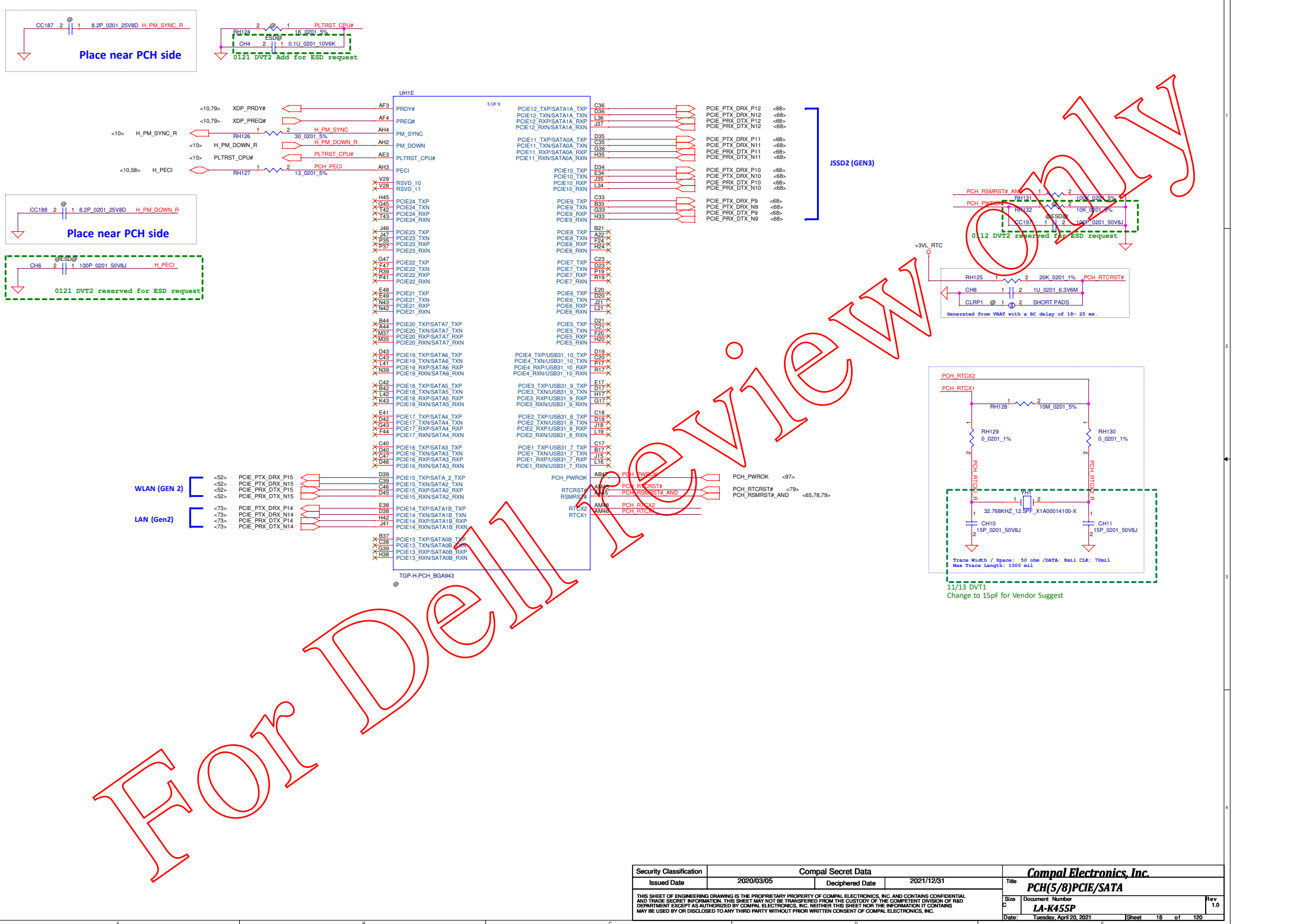


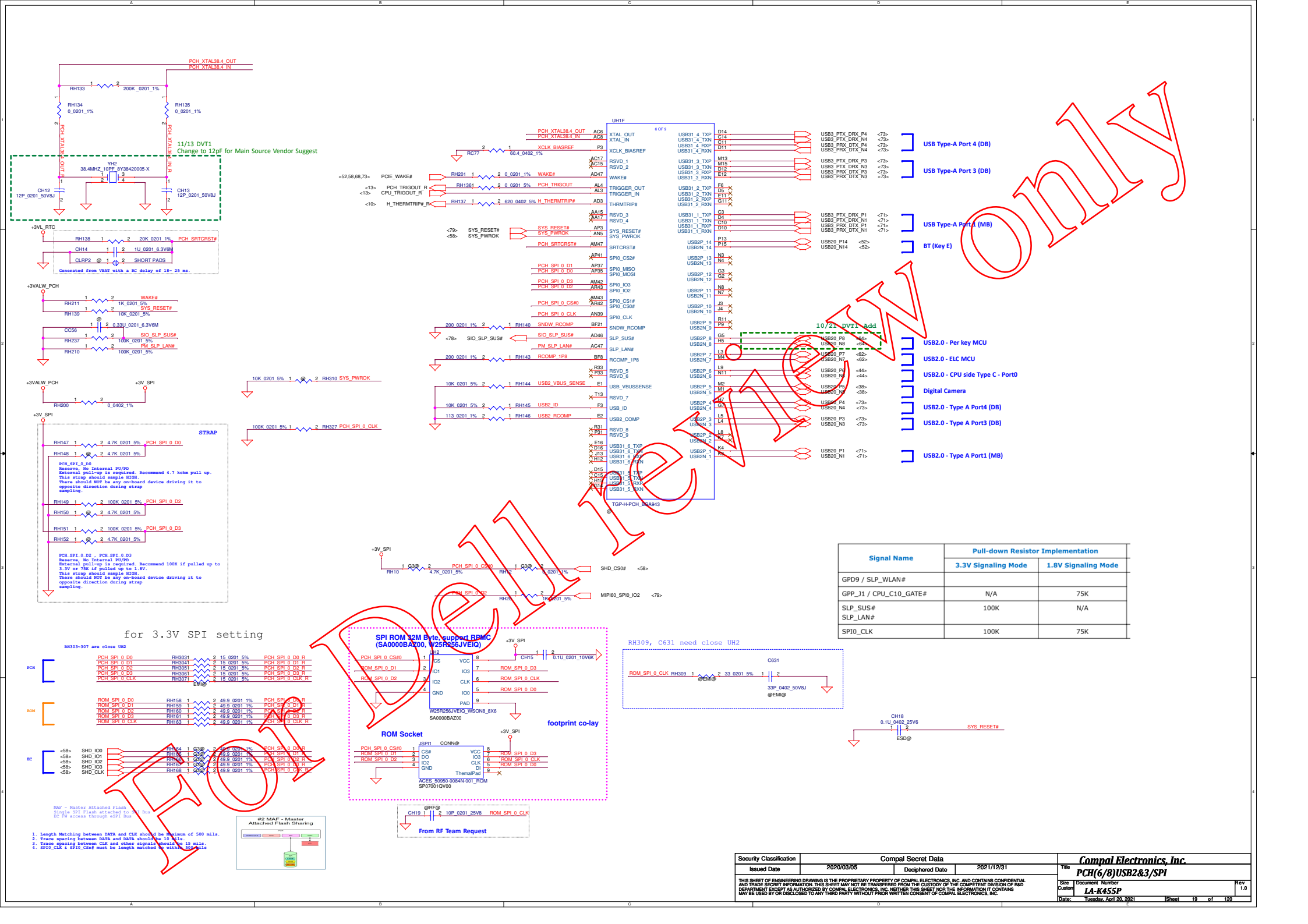
<58> SUSCLK_EC RH208 1 2 0.0201 1% SUSCLK
SUSCLK : RVP has one 33 ohm between PCH - JWLAN
0121 DVT2 stuff for ESD request

D Group 3.3V Only

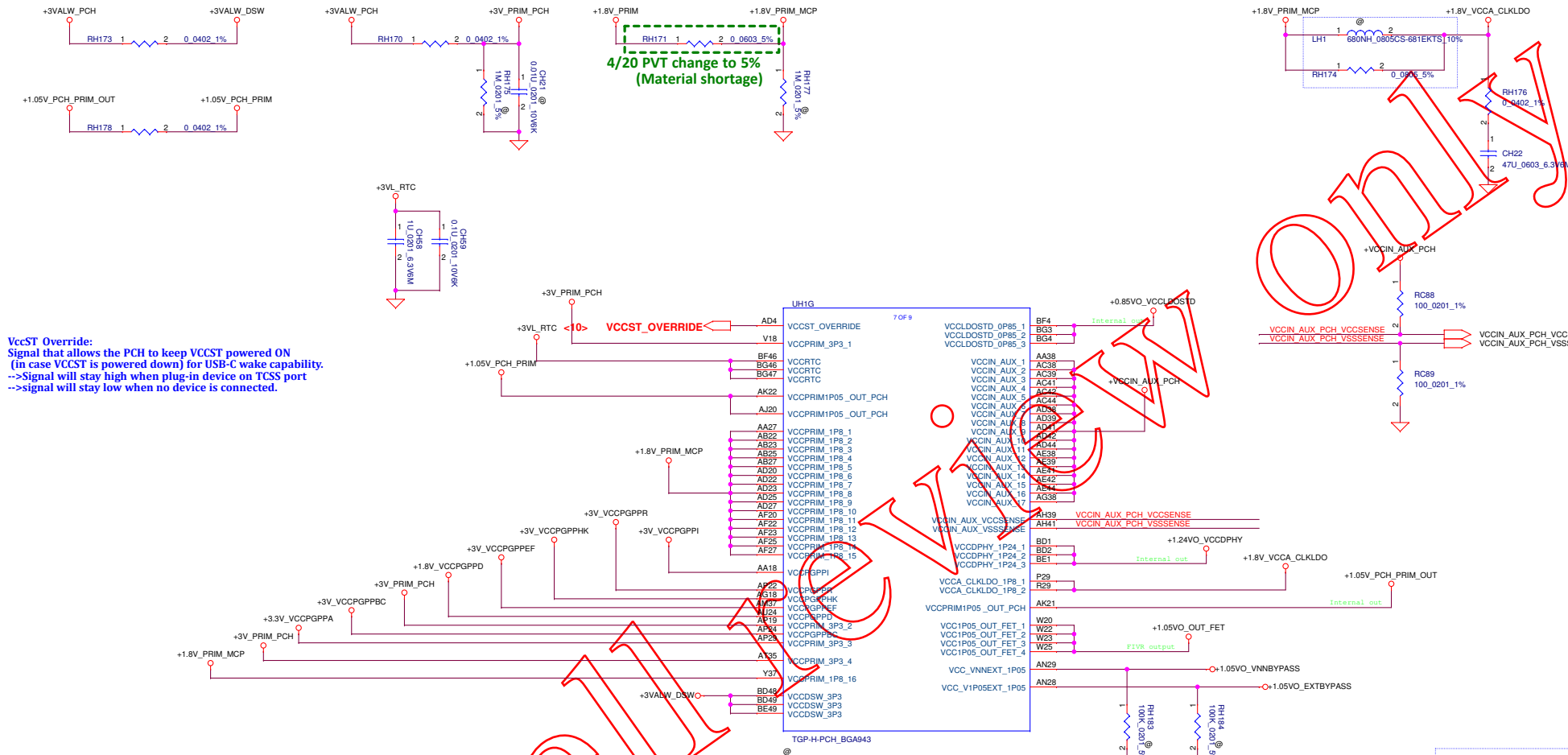


only





Check Current Value

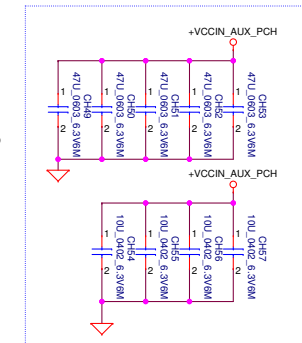
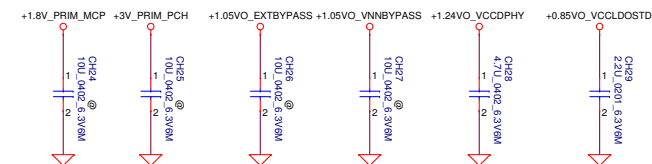
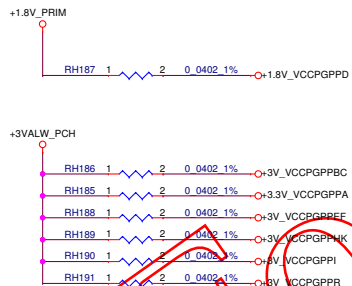


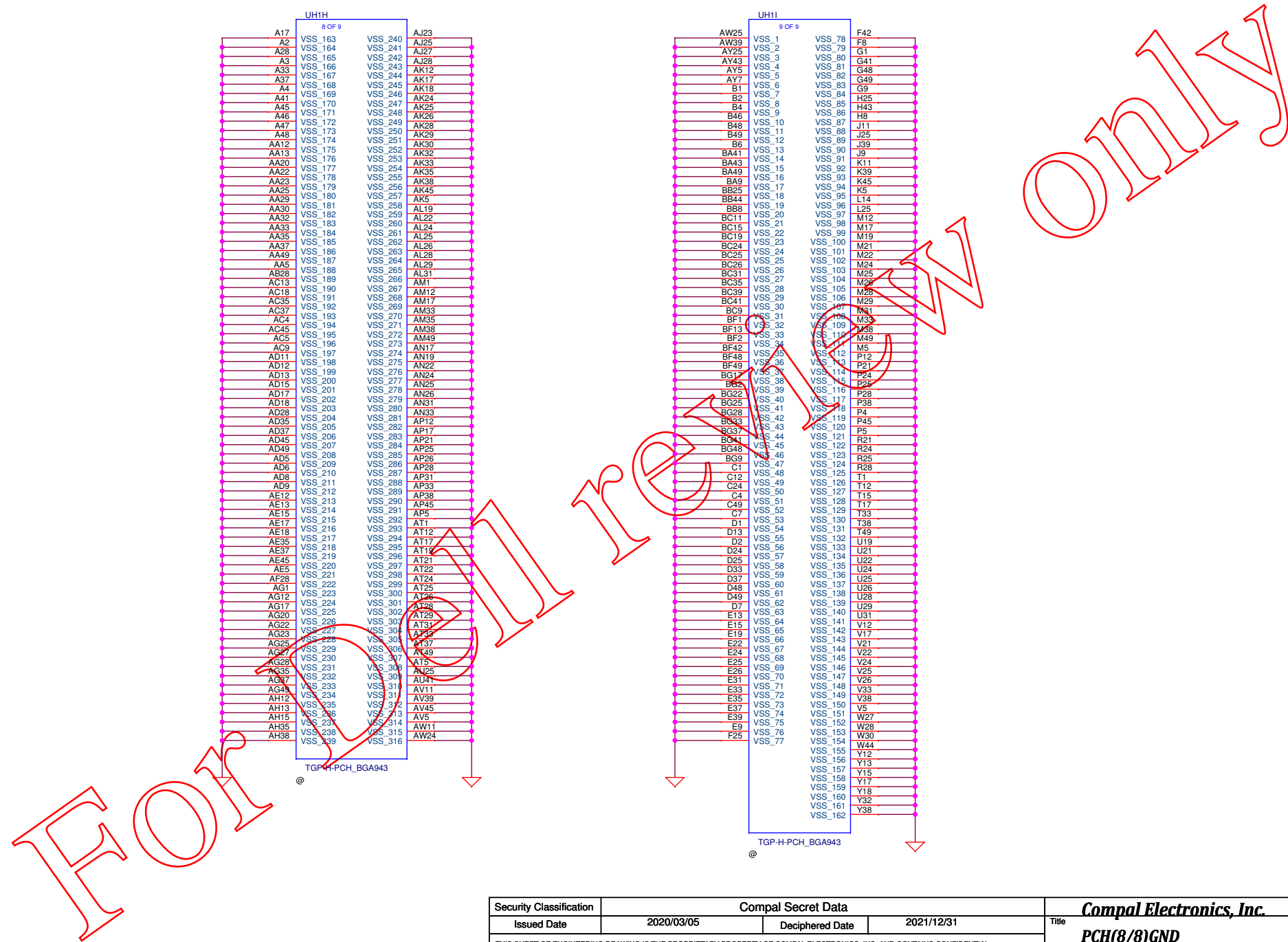
VccST Override:
Signal that allows the PCH to keep VCCST powered ON
(in case VCCST is powered down) for USB-C wake capability.
-->Signal will stay high when plug-in device on TCSS port
-->signal will stay low when no device is connected.

Table 28. GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPRIM_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V (Per-pad voltage configuration)
Primary Well Group B (GPP_B) Primary Well Group C (GPP_C)	VCCPGPPBC	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group D (GPP_D)	VCCPGPPD	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group E (GPP_E) Primary Well Group F (GPP_F)	VCCPGPPEF	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group G (GPP_G)	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V (Per-pad voltage configuration)
Primary Well Group H (GPP_H) Primary Well Group K (GPP_K)	VCCPGPHK	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group I (GPP_I)	VCCPGPI	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8 V Only
Primary Well Group R (GPP_R)	VCCPGPPR	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group S (GPP_S)	VCCPRIM_1P8	1.8 V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3 V Only

Note: For GPIO groups that support Per-group voltage configuration, the voltage is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage.
Note: For GPIO groups that support Per-pad voltage configuration, each pin voltage is selected by setting the corresponding voltage select soft strap of the pin.





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				Custom	LA-K455P
				Date:	Tuesday, April 20, 2021
				Sheet	21 of 120
				Rev	1.0

Main Function:

Reserve

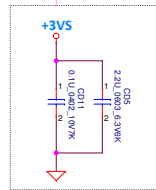
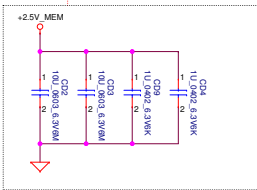
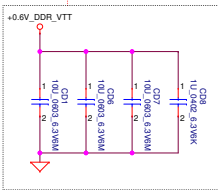
For Design Review Only

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2020/03/05	Deciphered Date	2019/04/01	Title	RSV	
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				Date:	Tuesday, April 20, 2021	Sheet 22 of 120

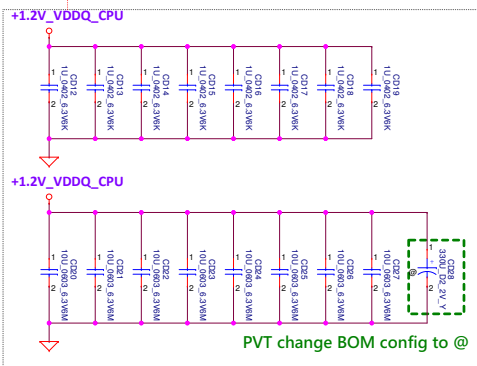
Layout Note:
Place near JDIM1.258

Layout Note:
Place near JDIMM1.257,259

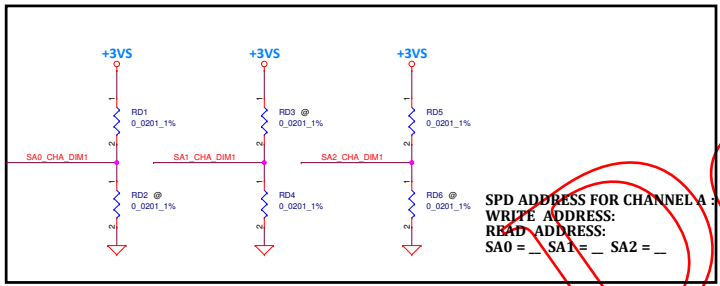
Layout Note:
Place near JDIMM1.255



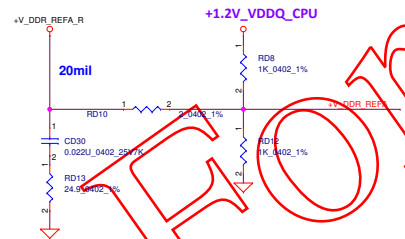
Layout Note:
Place near JDIMM1



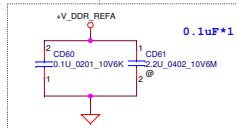
PVT change BOM config to @



SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS:
READ ADDRESS:
SA0 = _ SA1 = _ SA2 = _



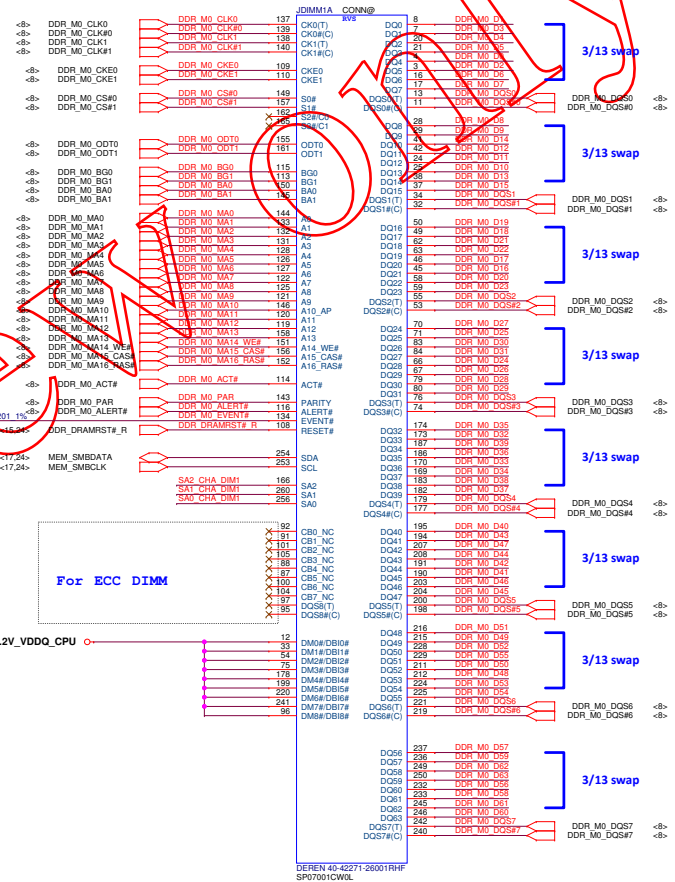
Layout Note:
PLACE THE CAP near JDIMM1. 164



Interleaved Memory

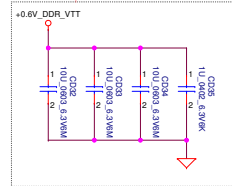


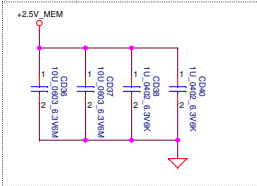
REVERSE TYPE (4 mm)

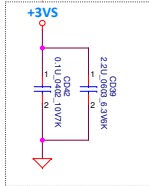


For ECC DIMM

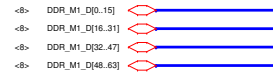
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Issued Date	2020/03/05	Deciphered Date	2017/01/08	Size		Rev 1.0
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				Drawing Number LA-K455P		
Date:				2021	Sheet	23 of 120



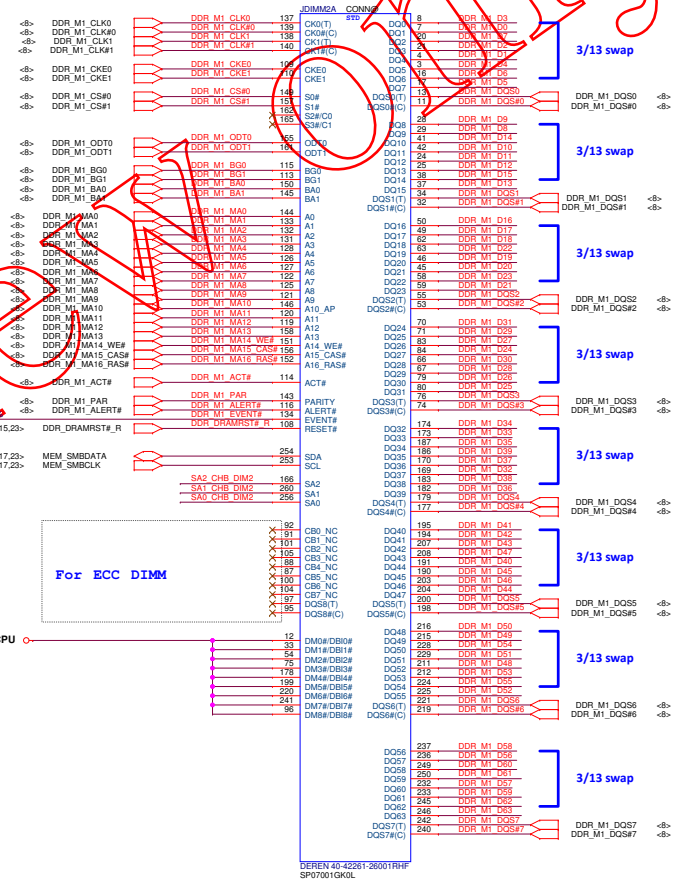
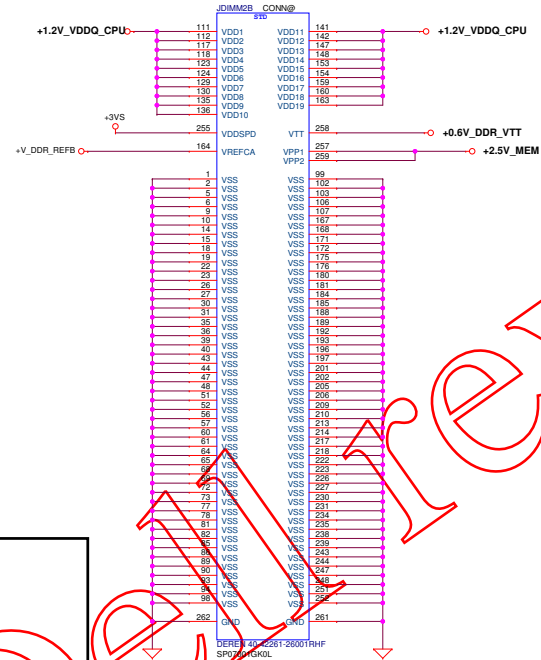
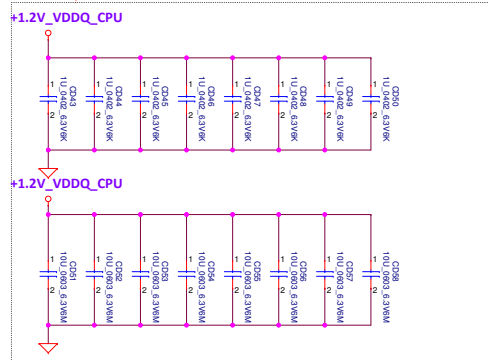




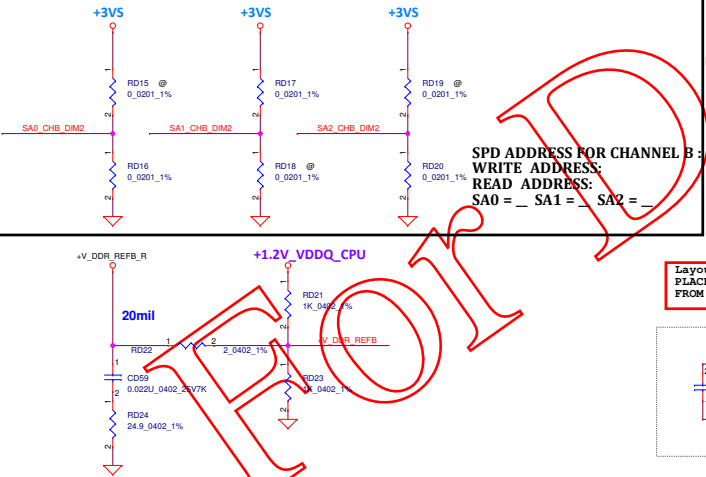
Interleaved Memory



STD (4 mm)

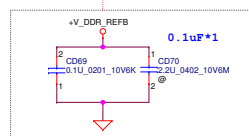


For ECC DIMM

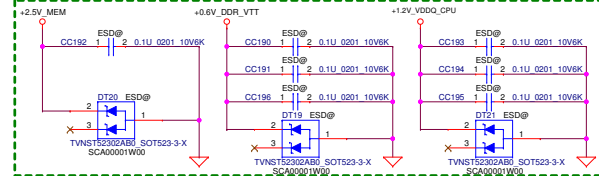


~~SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS:
READ ADDRESS:
SA0 = _ SA1 = _ SA2 = _~~

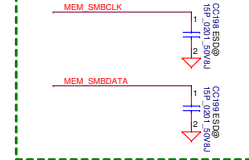
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2



```
0111 DVT2 add for ESD request
*****
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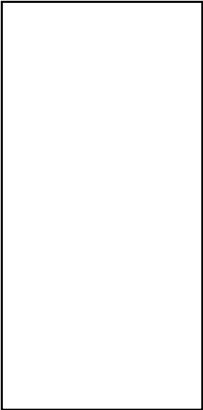


```
0112 DVT2 reserved for ESD request
0121 DVT2 stuff for ESD request
```



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Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title		
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				Model Number		1.0
				LA-K455P		
				Date:	Tuesday, Apr 20, 2021	Sheet 24 of 120

VRAM X76:

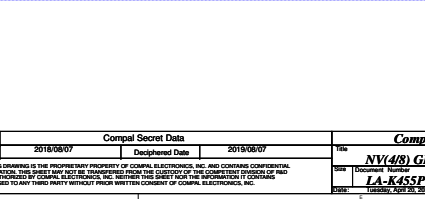
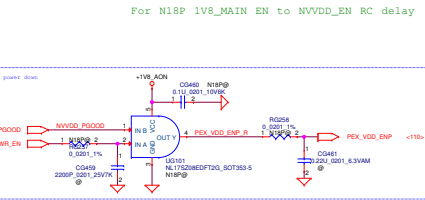
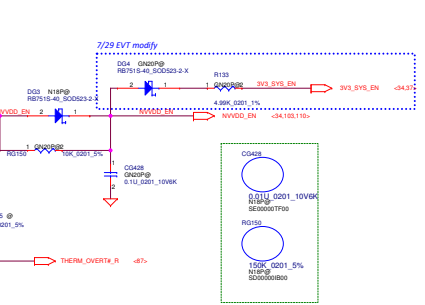
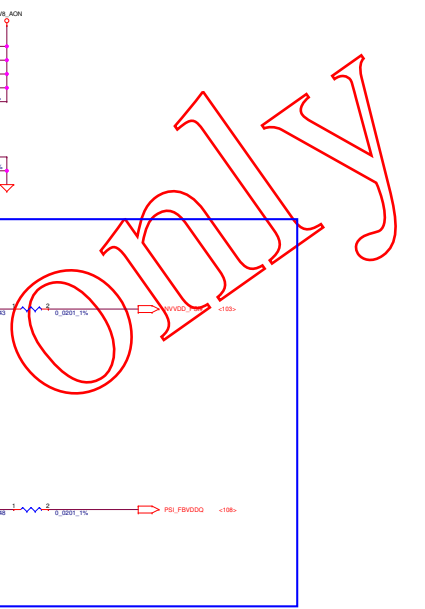
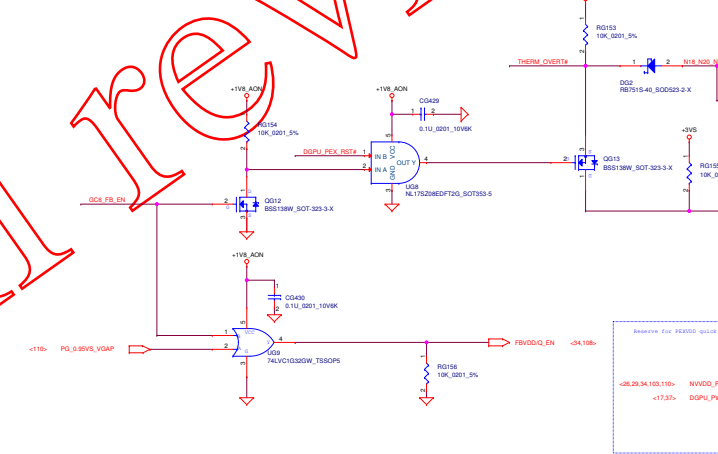
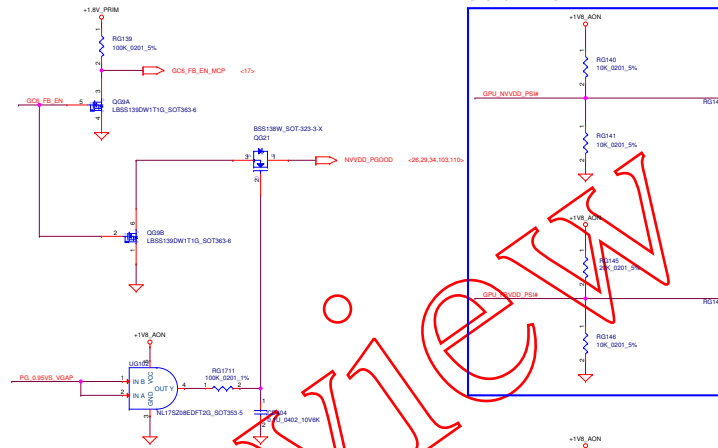
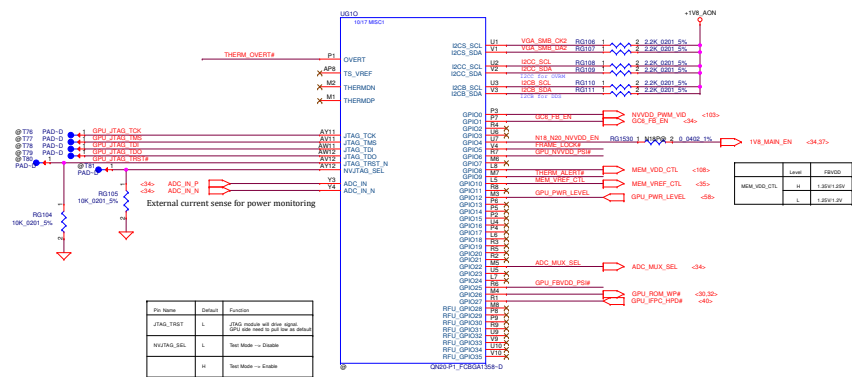


8G bit GDDR6					
Micron 4GB SKU		Samsung 4GB SKU		Hynix 4GB SKU	
R1	R3	R1	R3	R1	R3
	<div>UM8 V8RGR@</div> <div>M1T6T25AM2UE-14A1.2V</div> <div>SA0000D7L</div> <div>UM10 V8RGR@</div> <div>M1T1K25AM2UE-14A1.2V</div> <div>SA0000D7L</div> <div>UM11 V8RGR@</div> <div>M1T1K25AM2UE-14A1.2V</div> <div>SA0000D7L</div> <div>UM12 V8RGR@</div> <div>M1T1K25AM2UE-14A1.2V</div> <div>SA0000D7L</div> <div>RD86 V8M@</div> <div>100K ± 5% 0201</div> <div>SD43100385</div> <div>RD83 V8M@</div> <div>100K ± 5% 0201</div> <div>SD43100385</div> <div>RD85 V8M@</div> <div>100K ± 5% 0201</div> <div>SD43100385</div> <div>RD84 V8M@</div> <div>100K ± 5% 0201</div> <div>SD43100385</div>		<div>UM8 V8RGR@</div> <div>K4Z80325BC-HC14 1.2V</div> <div>SA0000C64L</div> <div>UM10 V8RGR@</div> <div>K4Z80325BC-HC14 1.2V</div> <div>SA0000C64L</div> <div>UM11 V8RGR@</div> <div>K4Z80325BC-HC14 1.2V</div> <div>SA0000C64L</div> <div>UM12 V8RGR@</div> <div>K4Z80325BC-HC14 1.2V</div> <div>SA0000C64L</div> <div>RD81 V5@</div> <div>100K ± 5% 0201</div> <div>SD43100385</div> <div>RD83 V5@</div> <div>100K ± 5% 0201</div> <div>SD43100385</div> <div>RD85 V5@</div> <div>100K ± 5% 0201</div> <div>SD43100385</div> <div>RD84 V5@</div> <div>100K ± 5% 0201</div> <div>SD43100385</div>		<div>UM8 V8RGR@</div> <div>H4G8C8E4AIR-S2C</div> <div>SA0000D7L</div> <div>UM10 V8RGR@</div> <div>H4G8C8E4AIR-S2C</div> <div>SA0000D7L</div> <div>UM11 V8RGR@</div> <div>H4G8C8E4AIR-S2C</div> <div>SA0000D7L</div> <div>UM12 V8RGR@</div> <div>H4G8C8E4AIR-S2C</div> <div>SA0000D7L</div> <div>RD81 V8M@</div> <div>100K ± 5% 0201</div> <div>SD43100385</div> <div>RD83 V8M@</div> <div>100K ± 5% 0201</div> <div>SD43100385</div> <div>RD85 V8M@</div> <div>100K ± 5% 0201</div> <div>SD43100385</div> <div>RD84 V8M@</div> <div>100K ± 5% 0201</div> <div>SD43100385</div>

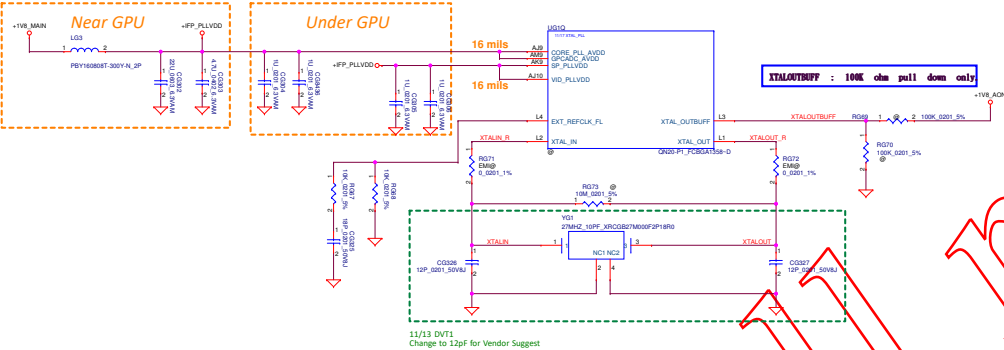
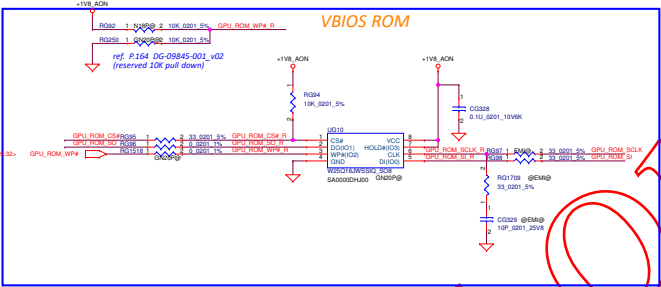
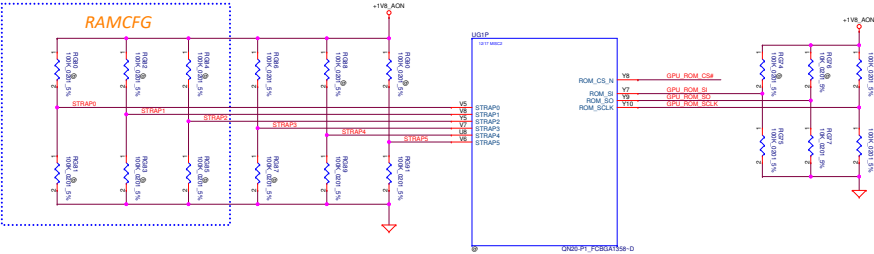
For Dell review only

For Dell review only





GDDR6 VRAM	Strap0	Strap1	Strap2
SAMSUNG	L	L	L
MICRON	H	L	L
HYNIX	L	H	L



STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
H	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

- 1:SMB_ALT_ADDR ENABLE
- 0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
- 0:DEVID_SEL ORIGINAL
- 1:PCIE_CFG LOW POWER
- 0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
- 0:VGA_DEVICE DISABLE

Default

For Detailed Review Only

UG1D		UG1E	
15/17 GND_12		16/17 GND_23	
A10	GND 001	AN10	GND 001
A2	GND 002	AN2	GND 002
A3	GND 003	AN3	GND 003
A31	GND 004	AN34	GND 004
A34	GND 005	AN35	GND 005
A37	GND 006	AN39	GND 006
A39	GND 007	AN4	GND 007
A4	GND 008	AP12	GND 008
A7	GND 009	AP14	GND 009
AB13	GND 010	AP16	GND 010
AB14	GND 011	AP18	GND 011
AB15	GND 012	AP20	GND 012
AB16	GND 013	AP22	GND 013
AB17	GND 014	AP24	GND 014
AB18	GND 015	AP26	GND 015
AB19	GND 016	AP28	GND 016
AB21	GND 017	AP32	GND 017
AB22	GND 018	AP37	GND 018
AB23	GND 019	AP4	GND 019
AB24	GND 020	AP40	GND 020
AB25	GND 021	AP6	GND 021
AB26	GND 022	AP10	GND 022
AB27	GND 023	AP11	GND 023
AB28	GND 024	AP13	GND 024
AB31	GND 025	AP15	GND 025
AB32	GND 026	AP17	GND 026
AD13	GND 027	AP19	GND 027
AD14	GND 028	AP21	GND 028
AD15	GND 029	AP23	GND 029
AD16	GND 030	AP25	GND 030
AD17	GND 031	AP27	GND 031
AD18	GND 032	AP29	GND 032
AD19	GND 033	AP31	GND 033
AD20	GND 034	AP33	GND 034
AD21	GND 035	AP34	GND 035
AD22	GND 036	AP35	GND 036
AD23	GND 037	AP39	GND 037
AD24	GND 038	AP4	GND 038
AD25	GND 039	AP7	GND 039
AD26	GND 040	AT11	GND 040
AD27	GND 041	AT32	GND 041
AD28	GND 042	AT33	GND 042
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AE32	GND 044	AT37	GND 044
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AF14	GND 046	AT4	GND 046
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AF16	GND 048	AU12	GND 048
AF17	GND 049	AU13	GND 049
AF18	GND 050	AU14	GND 050
AF19	GND 051	AU15	GND 051
AF20	GND 052	AU16	GND 052
AF21	GND 053	AU17	GND 053
AF22	GND 054	AU18	GND 054
AF23	GND 055	AU19	GND 055
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AF25	GND 057	AU20	GND 057
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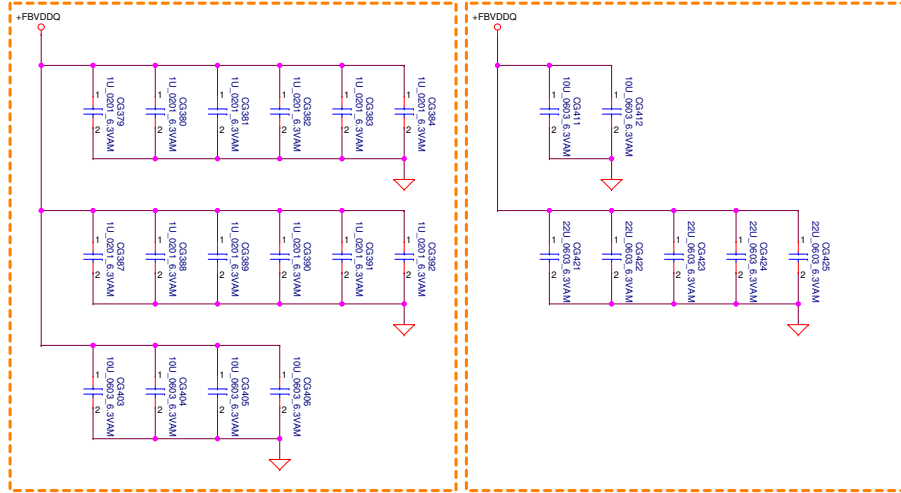
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				Size	
				Document Number	
				LA-K455P	
				Rev	
				1.0	
				Date: Tuesday, April 20, 2021	
				Sheet 31 of 120	

FBVDDQ_GPU

Under GPU

Near GPU



Only

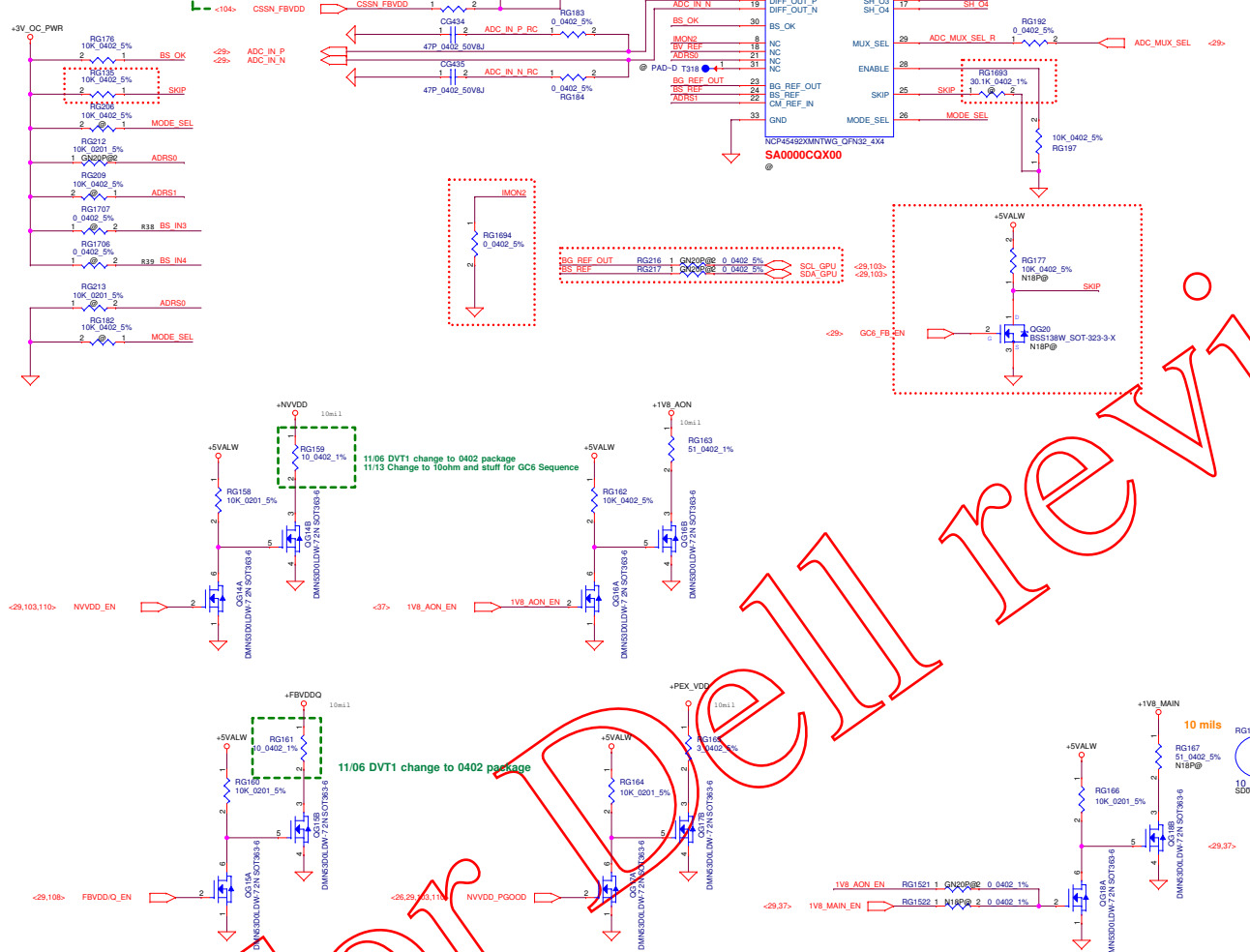
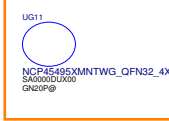
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				Tuesday, April 20, 2021	1.0
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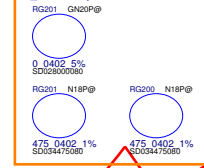
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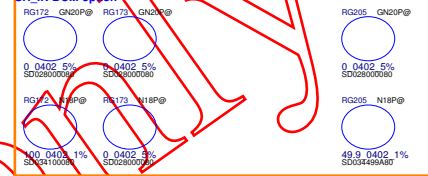
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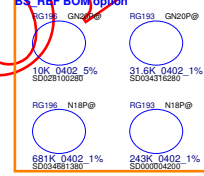
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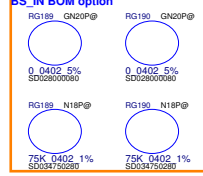
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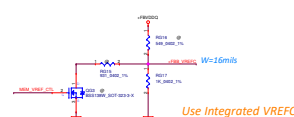
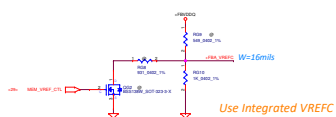
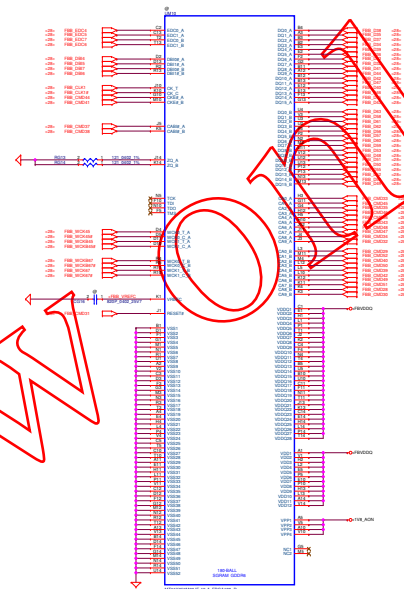
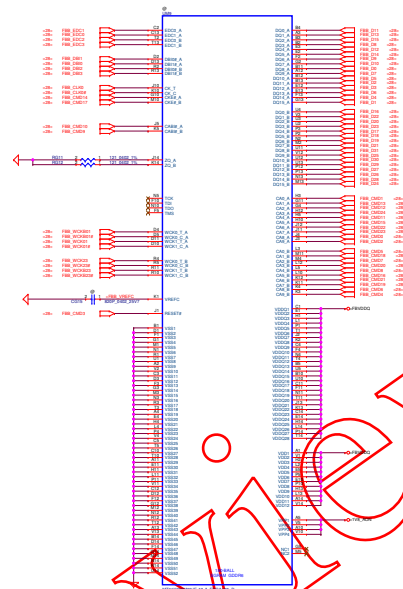
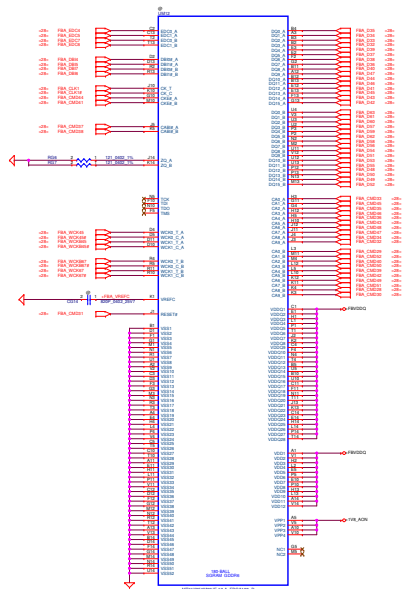
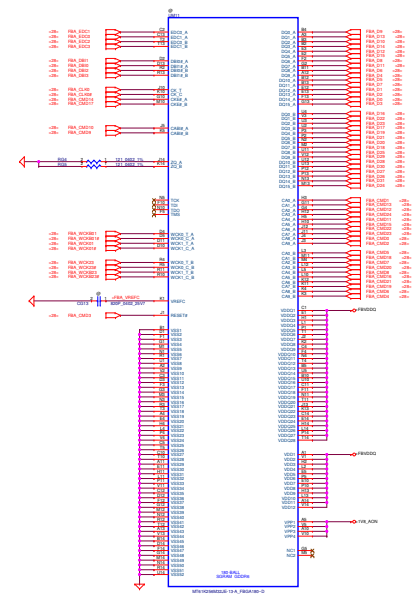
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				L4-K455P	
				Date:	10/25/2017, April 20, 2021
				Sheet	34 of 139

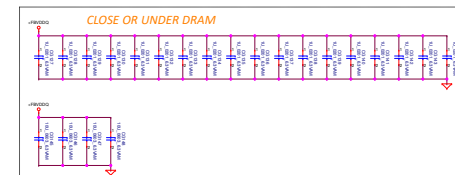
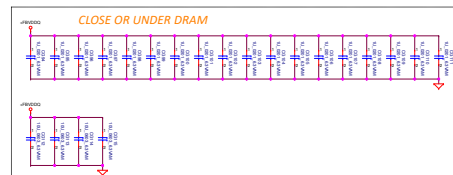
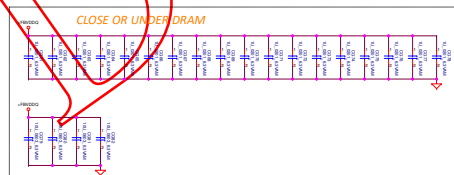
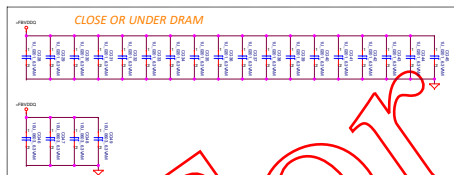
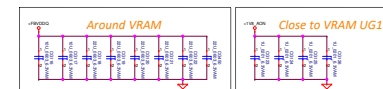
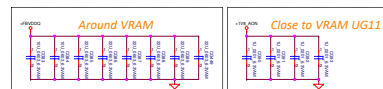
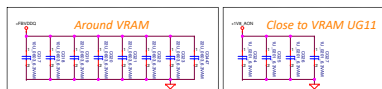


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UM12

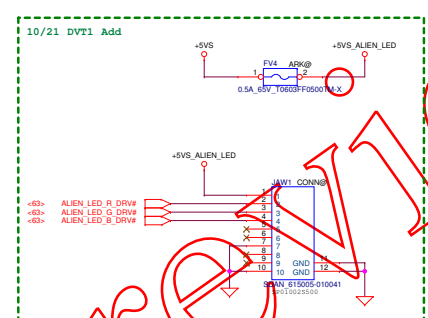
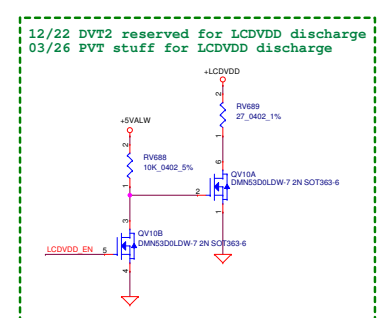
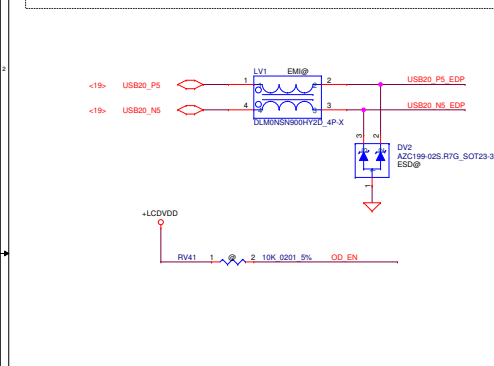
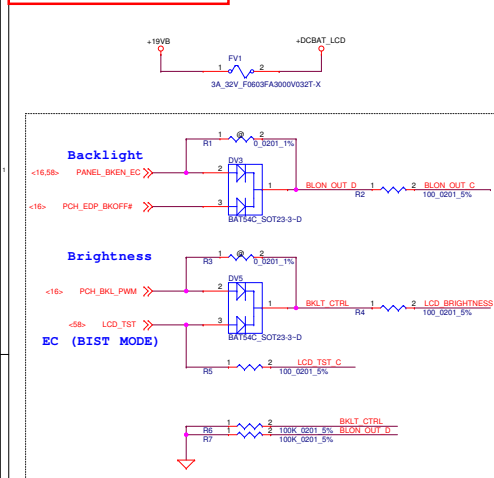
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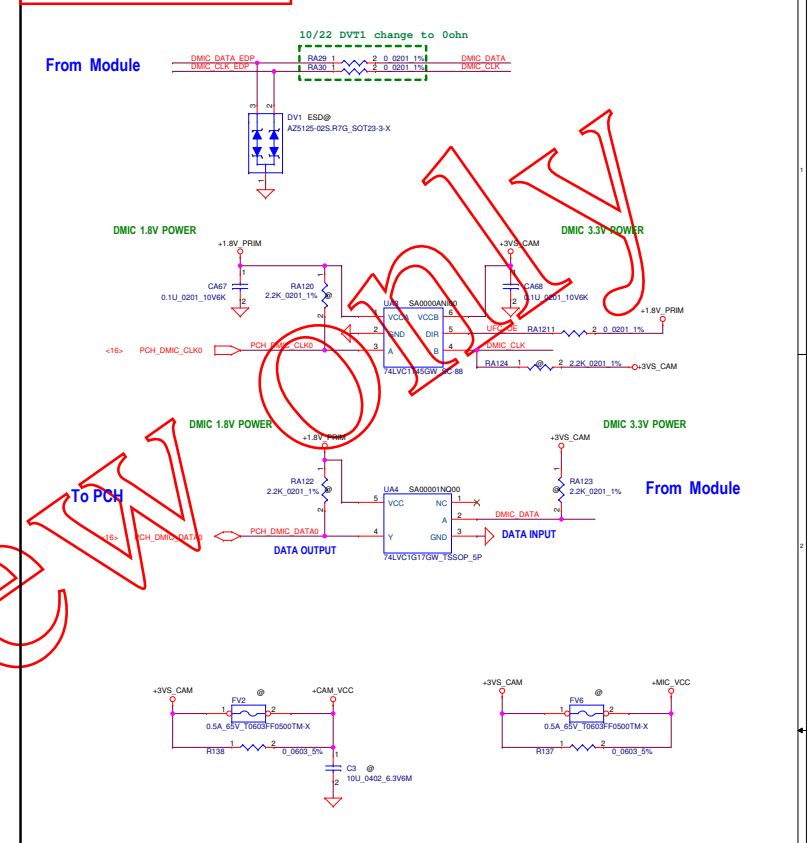


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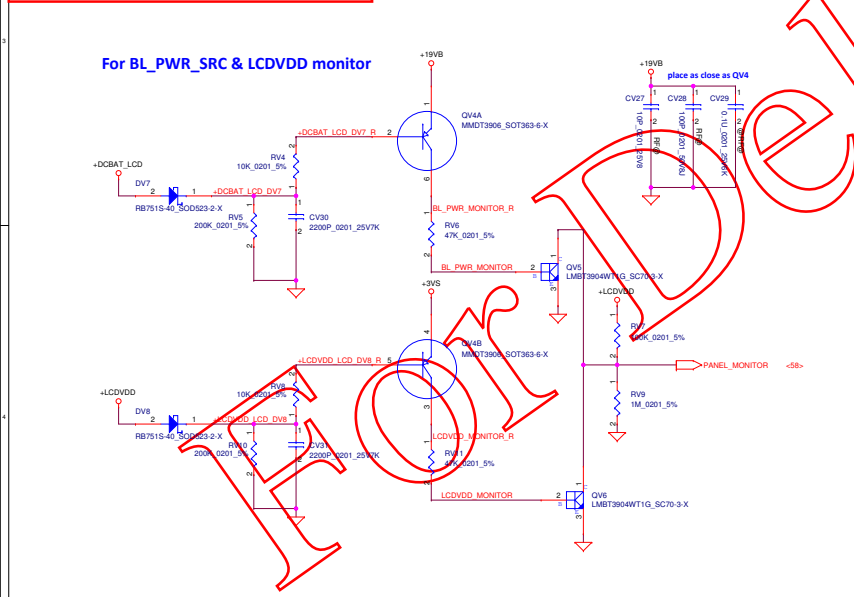
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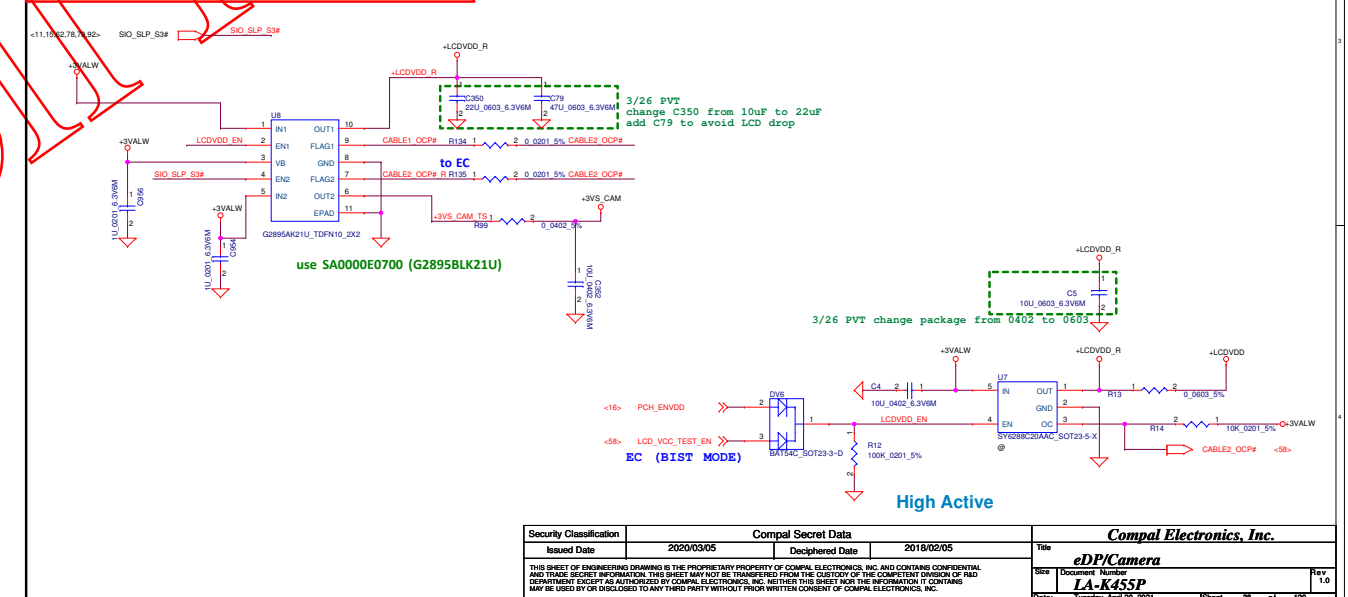
Main Func = DMIC



Main Func = LCDVDD monitor



Main Func = Hinge up protection



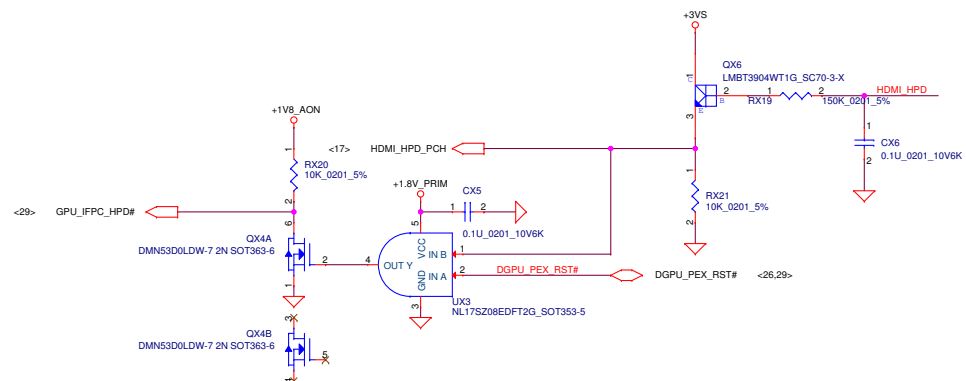
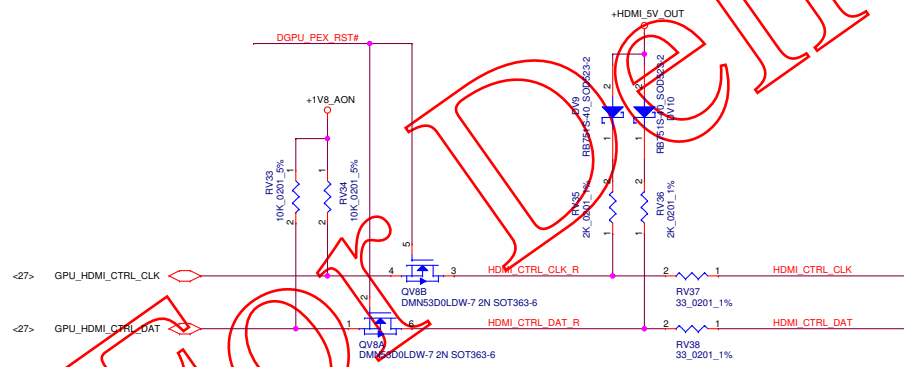
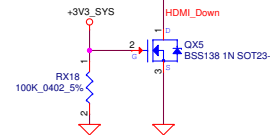
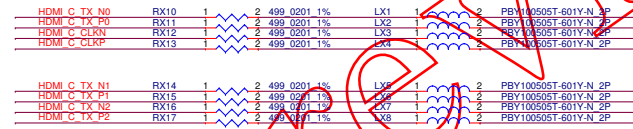
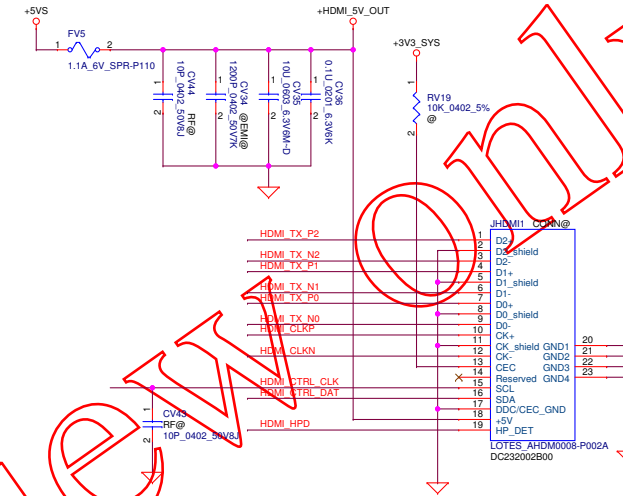
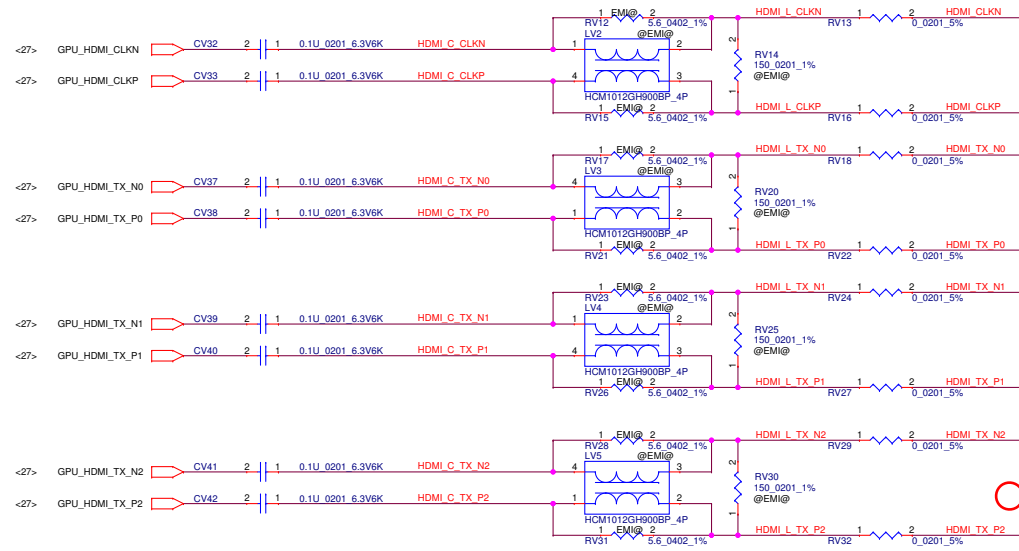
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Issued Date	2020/03/05	Deciphered Date		2018/02/05	Title	eDP/Camera	
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Main Func = DDS

Main Func = eDP MUX

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				Draw	Tuesday, Feb 20, 2021
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Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		HDMI	
2020/03/05		2018/02/05		Document Number	
				LA-K455P	
				Date: Tuesday, April 20, 2021	
				Sheet 40 of 120	

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				Sheet 43 of 120		

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				Date:	LA-K455P	1.0
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				Date:	LA-K455P	1.0
				Tuesday, April 20, 2021	Sheet 53 of 120	

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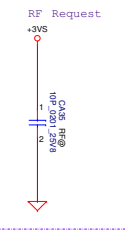
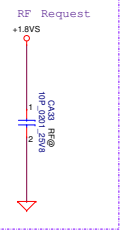
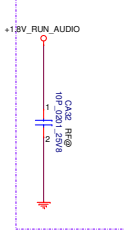
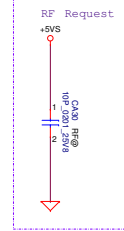
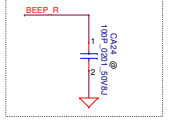
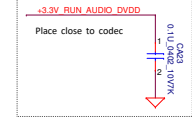
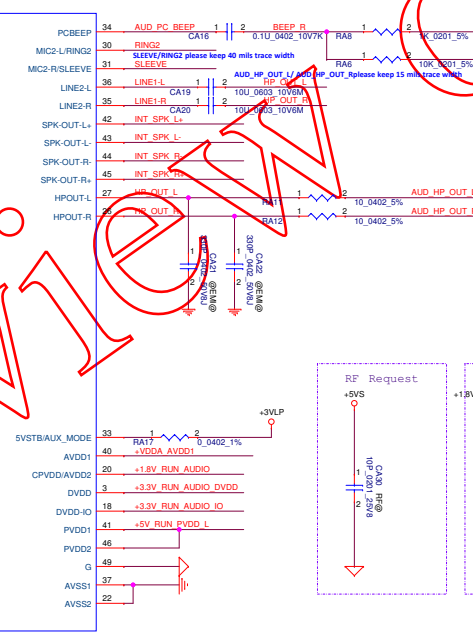
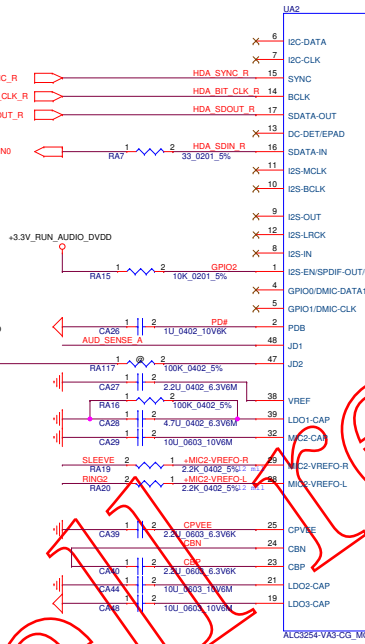
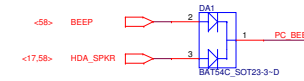
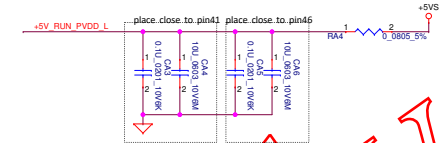
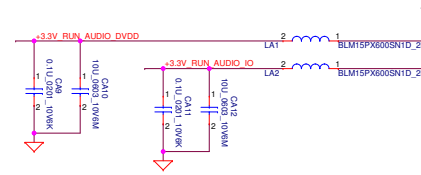
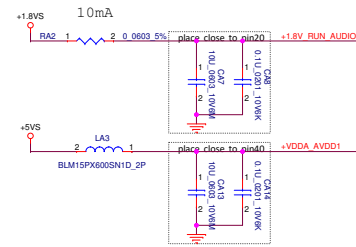
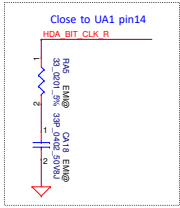
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	RSV	
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Main Function:

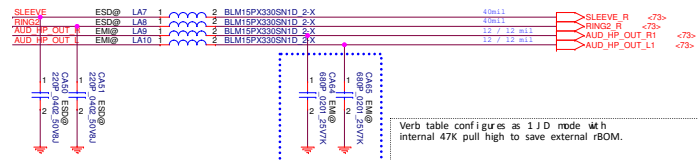
Reserve

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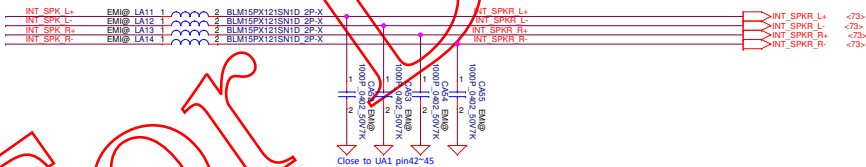
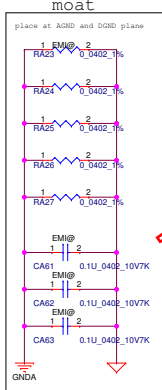
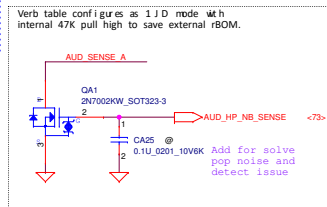
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Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	RSV	
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Place CAP and ESD Diode on DB



8/17 modify to 680pF for EMI request



Close to UA1 pin42-45

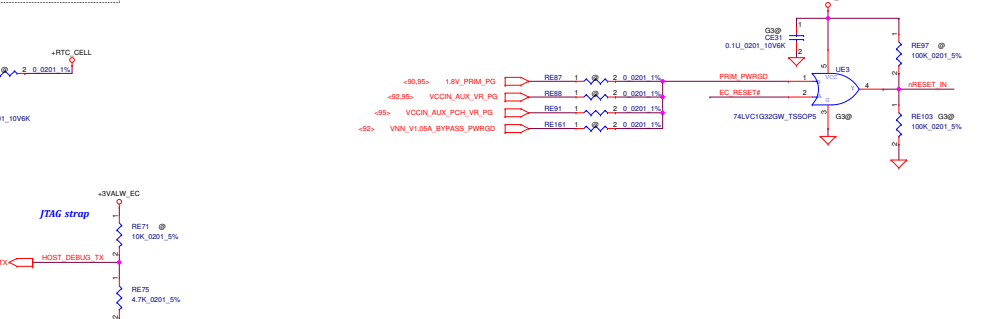
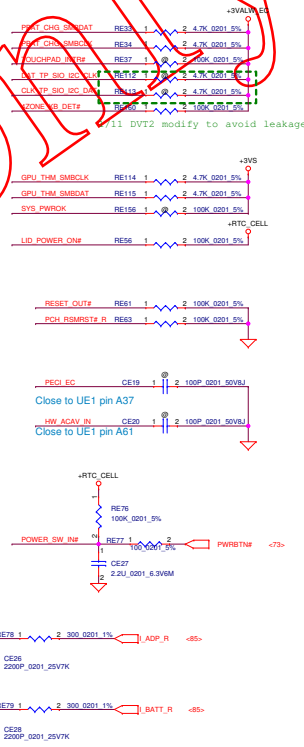
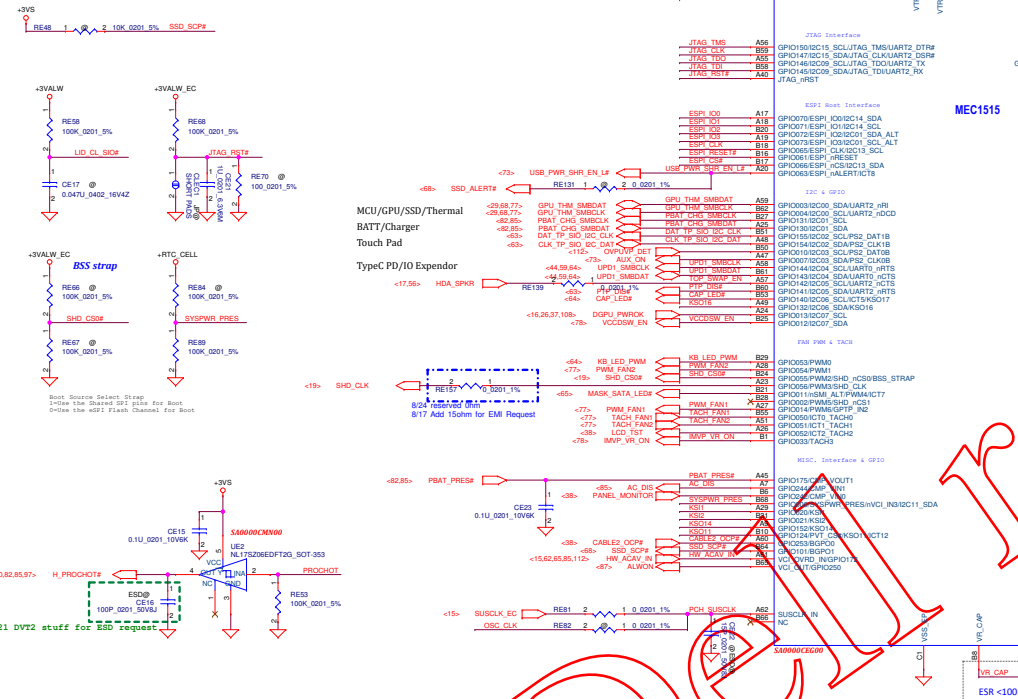
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Issued Date		Deciphered Date		Title	
2020/03/05		2018/10/01		Audio Codec ALC3254	
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Date:		Tuesday, April 20, 2021		Sheet 56 of 120	

Main Function:

Reserve

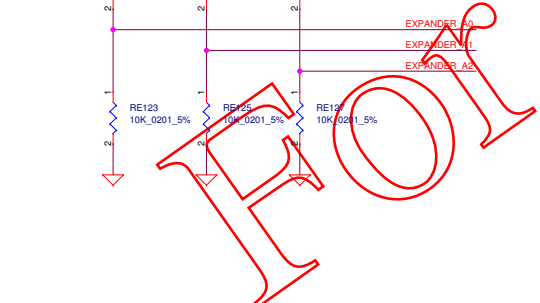
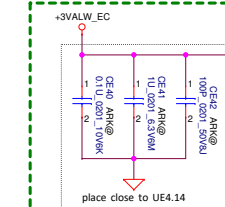
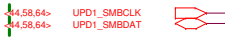
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Date				Issue	Sheet	58 of 21 120

R/W = 0 = Write
R/W = 1 = Read
SMBus address 0x40



INPUTS			OUTPUTS Q
CLR	\bar{A}	B	
L	X	X	L
X	H	X	L ⁽¹⁾
X	X	L	L ⁽¹⁾
H	L	↑	
H	↓	H	
↑	L	H	



Main Function:

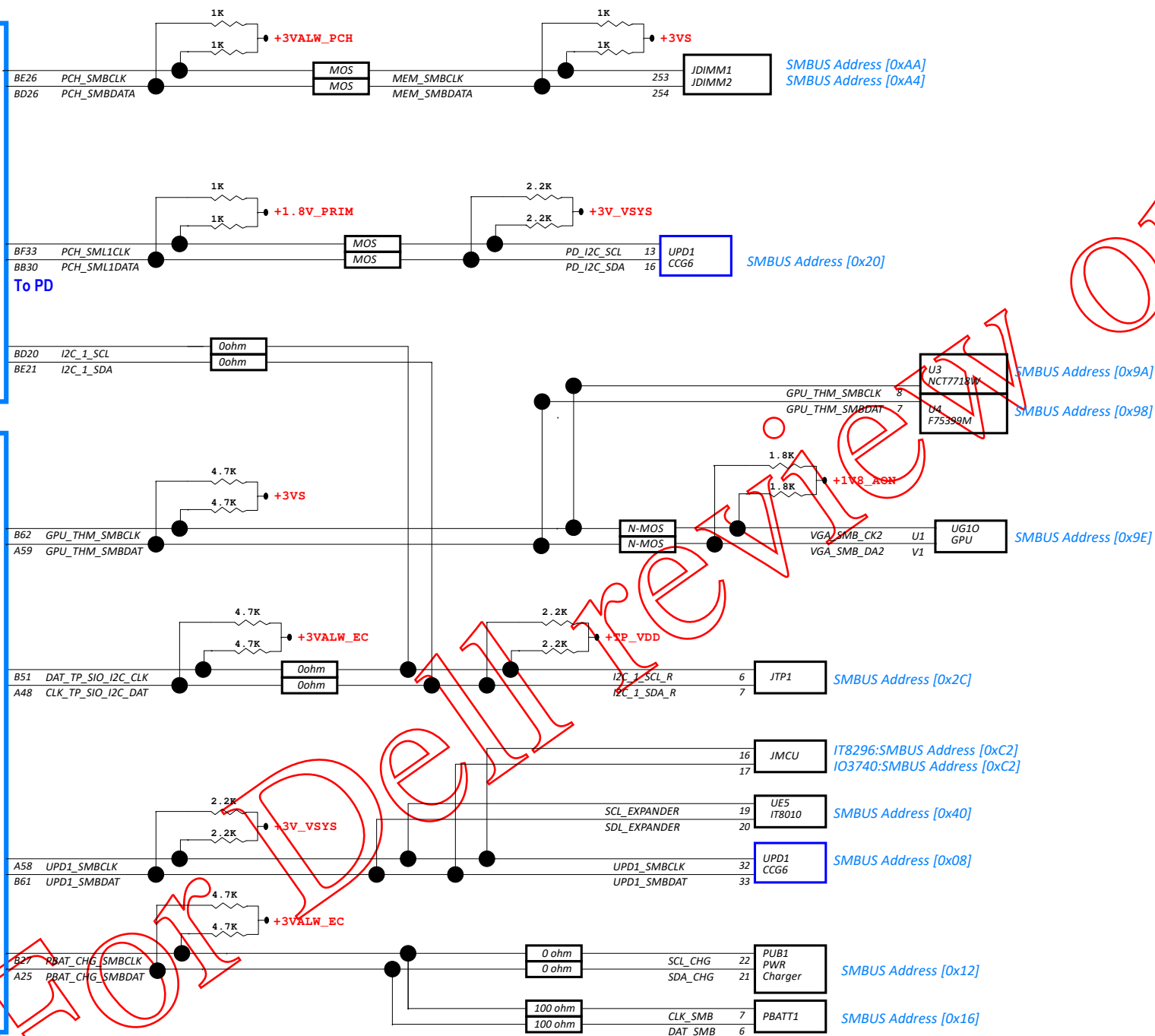
Reserve

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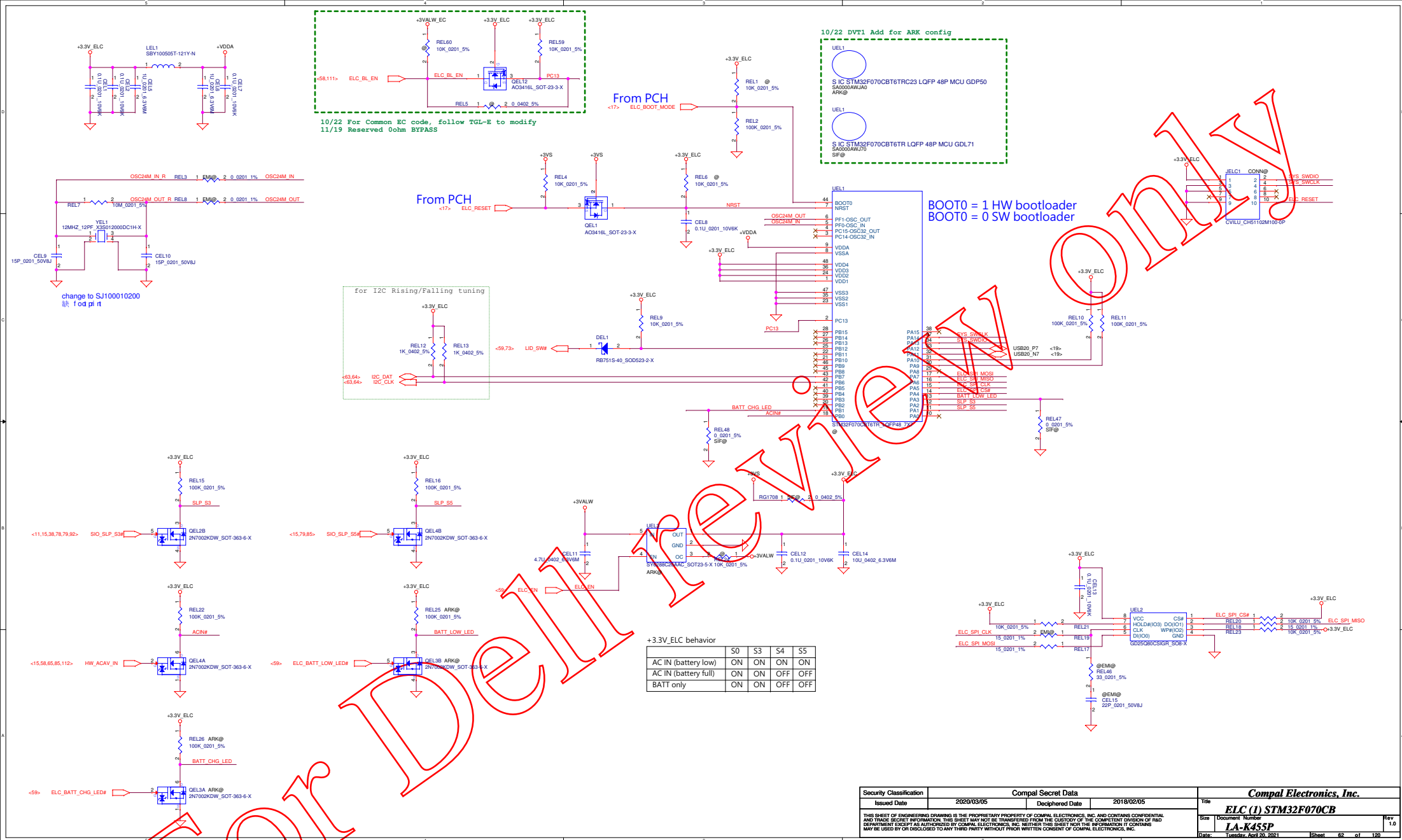
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Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	RSV	
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Tiger Lake
PCH-H

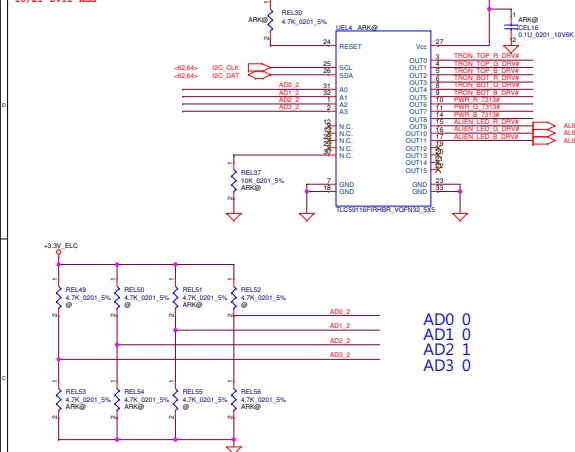
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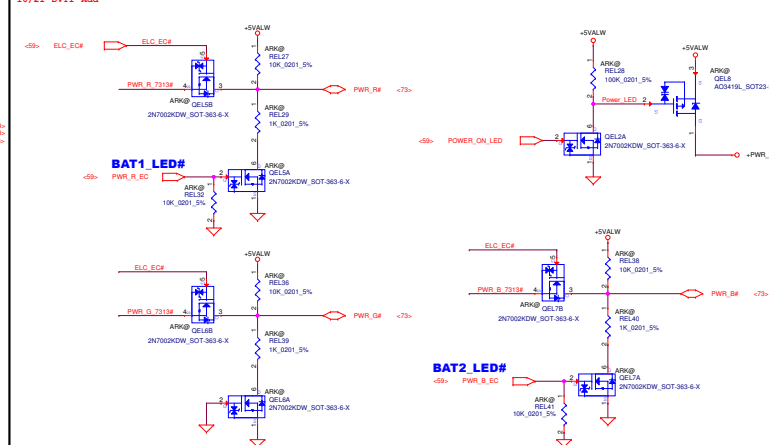
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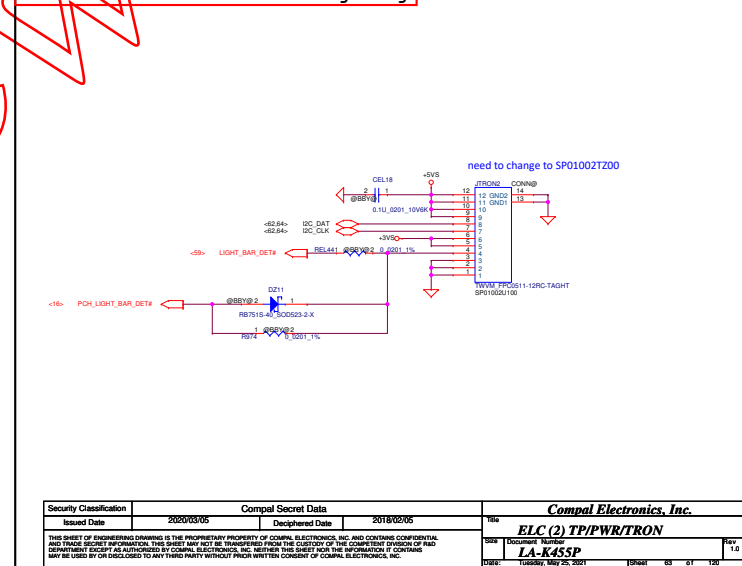
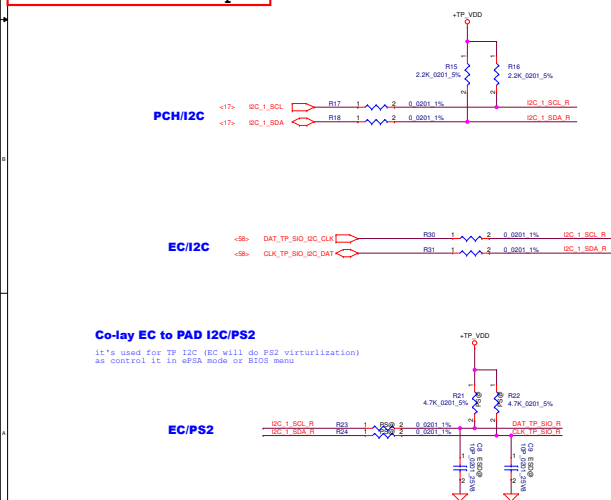
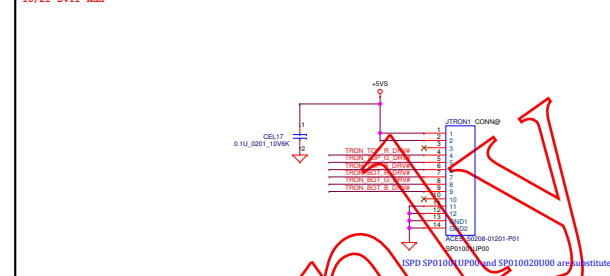
10/21 DVT1 Add



10/21 DVT1 Add



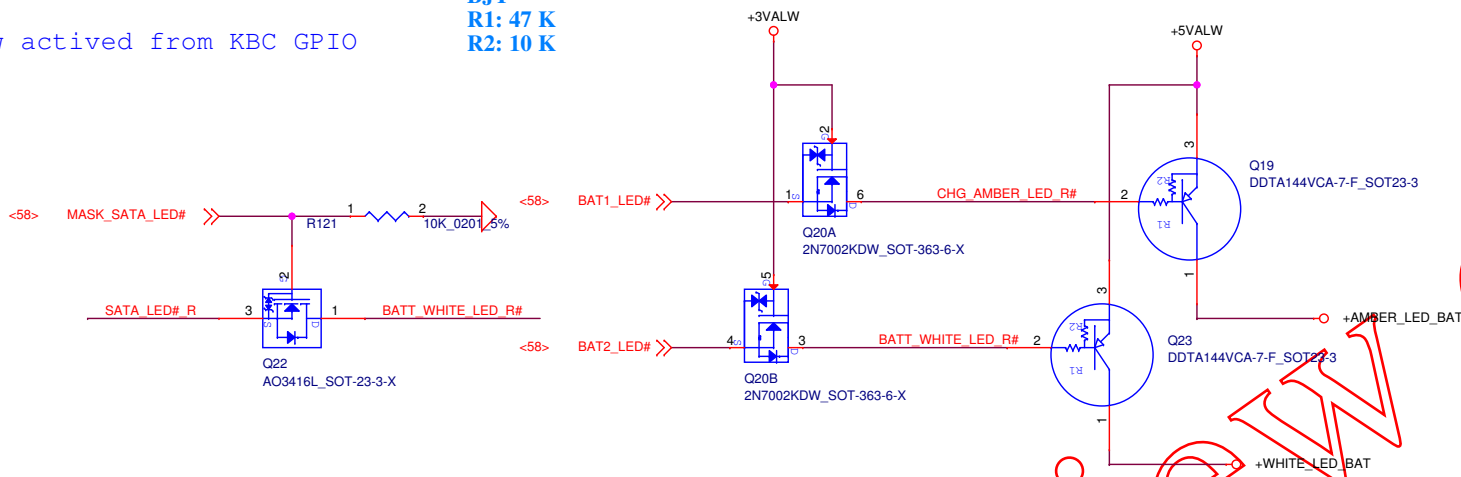
10/21 DVT1 Add



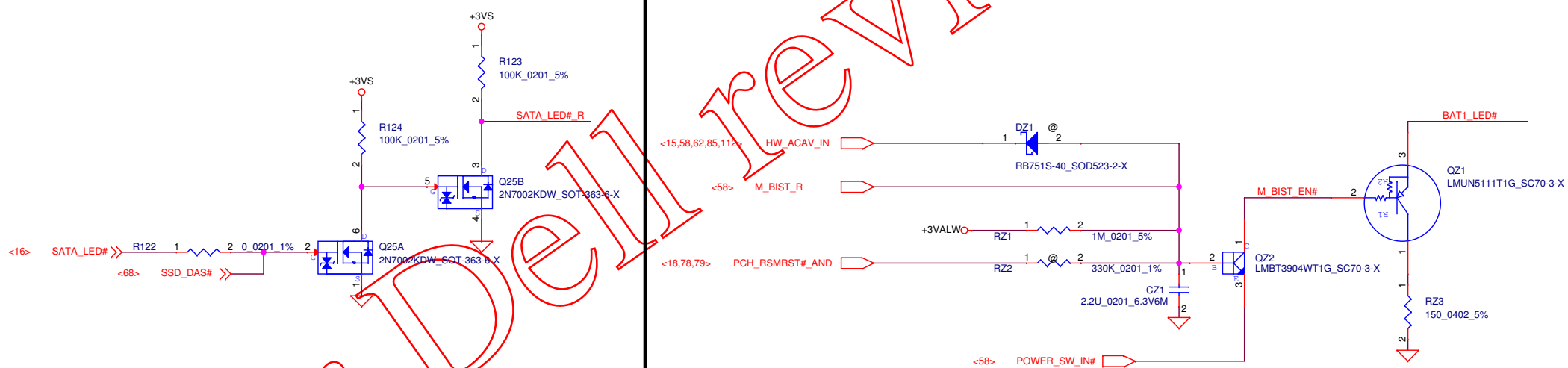
Main Func = Battery LED

Low actived from KBC GPIO

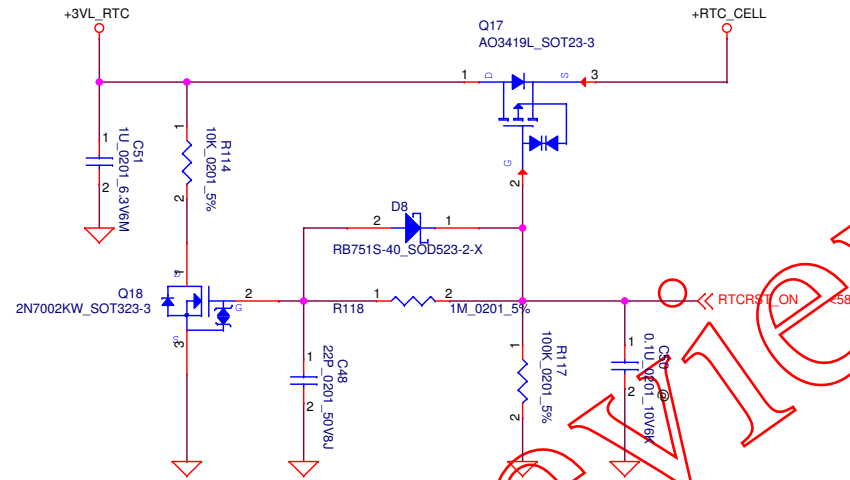
BJT
R1: 47 K
R2: 10 K



Main Func = M_BIST



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				Size	Document Number
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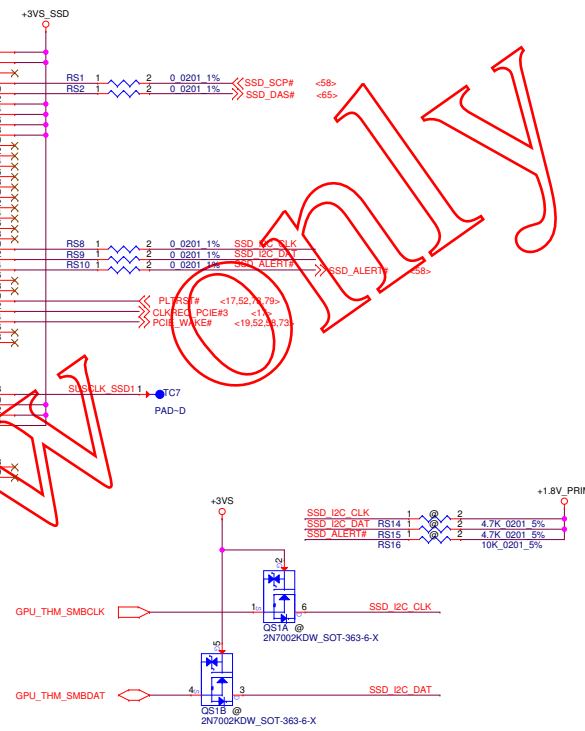
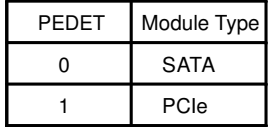
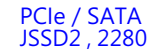
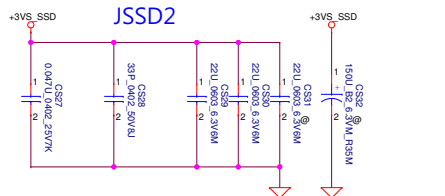
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Issued Date	2020/03/05	Deciphered Date	2019/04/01	Title	
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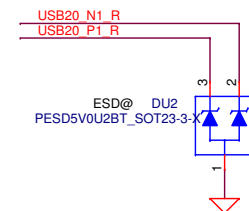
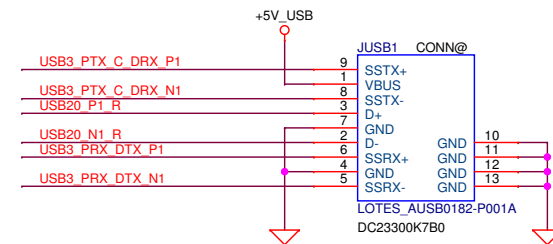
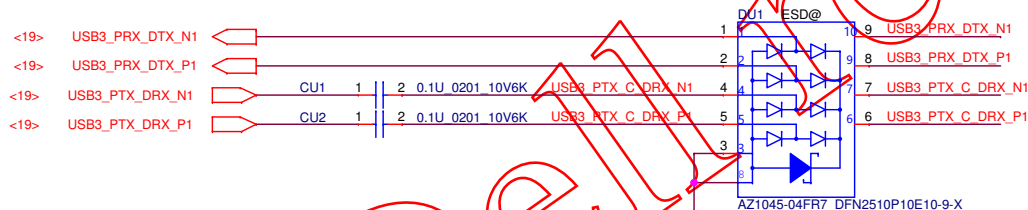
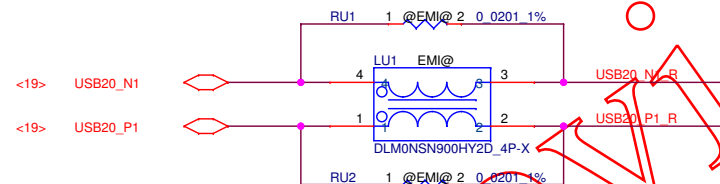
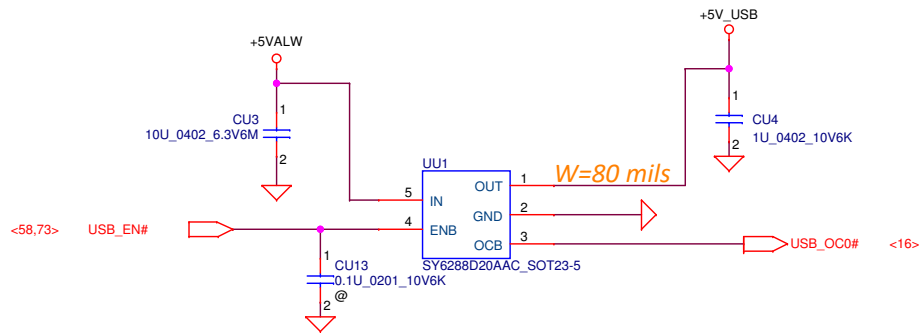
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Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	RSV	
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				Size	Rev
				Document Number	1.0
				LA-K455P	
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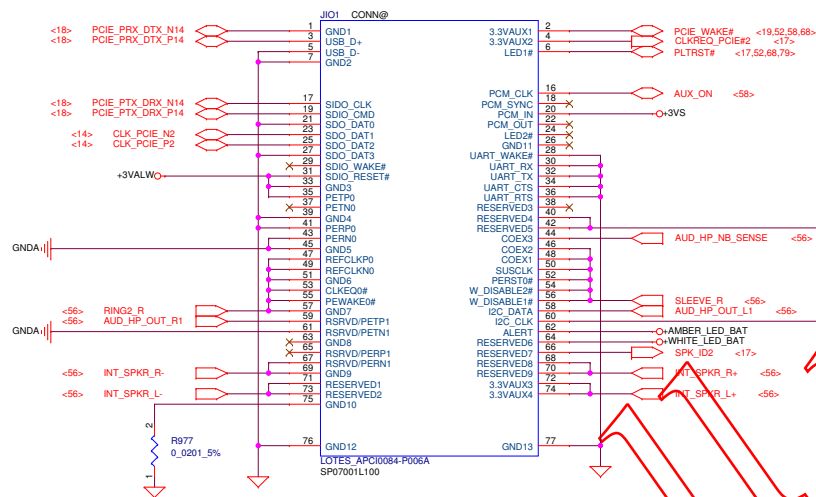
Main Function:

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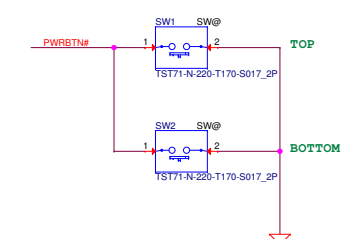
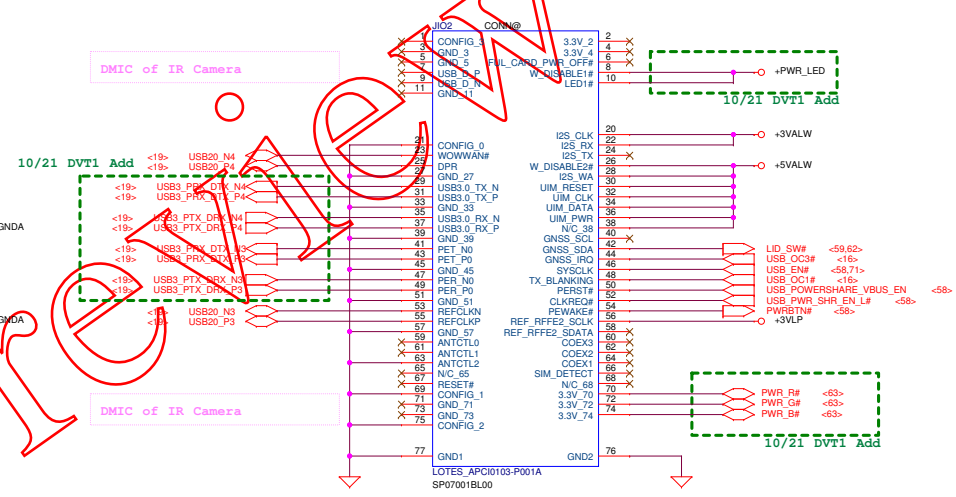
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A Key CONN



B Key CONN

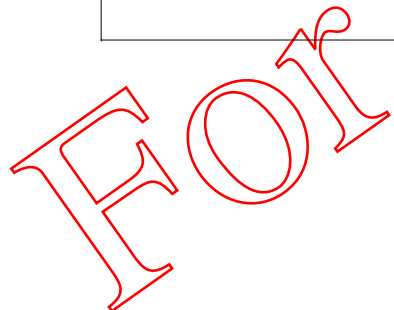


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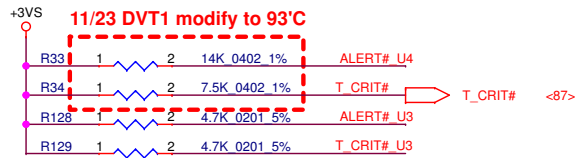


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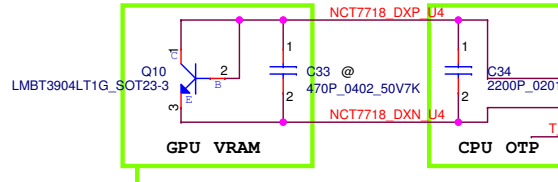
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Address 1001100xb (0x98h)

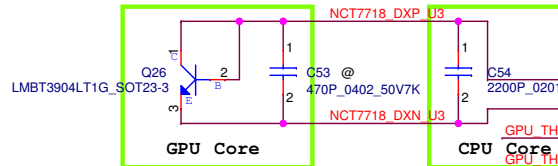


Layout Note:

Layout Note:
C34 close U4

DXN and DXP routing width and spacing is 10 mil / 10 mil.

Address 1001101xb (0x9Ah)



Layout Note:

Layout Note:
C54 close U3

DXN and DXP routing width and spacing is 10 mil / 10 mil.

CPU FAN Control

<58> PWM_FAN1
 <58> TACH_FAN1

GPU FAN Control

<58> PWM_FAN2
 <58> TACH_FAN2

11/4 DVT1 modify for material preparation on SCS00009500 change to SCS00000200

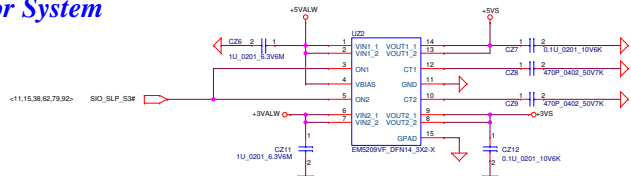
11/4 DVT1 modify for material preparation on SCS00009500 change to SCS00000200

03/22 PVT modify to short pad

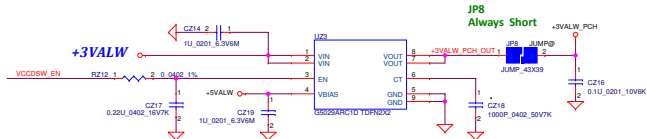
TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

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				Sheet	77 of 120

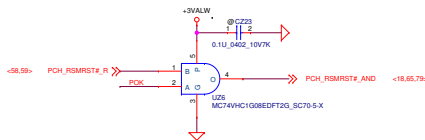
+5VS / +3VS for System



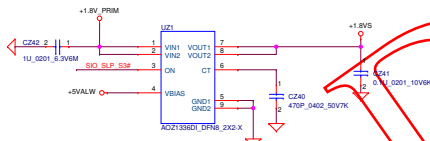
+3VALW TO +3VALW_PCH



RSMRST circuit

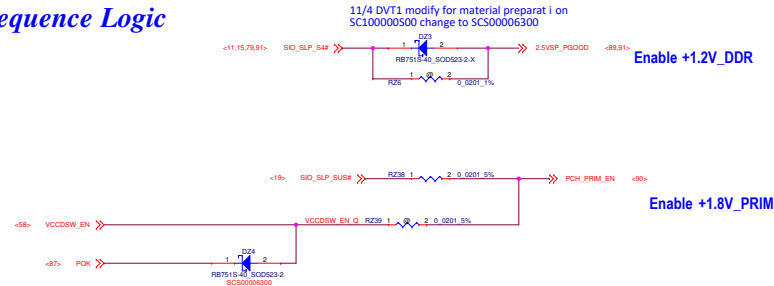


+1.8VS for System

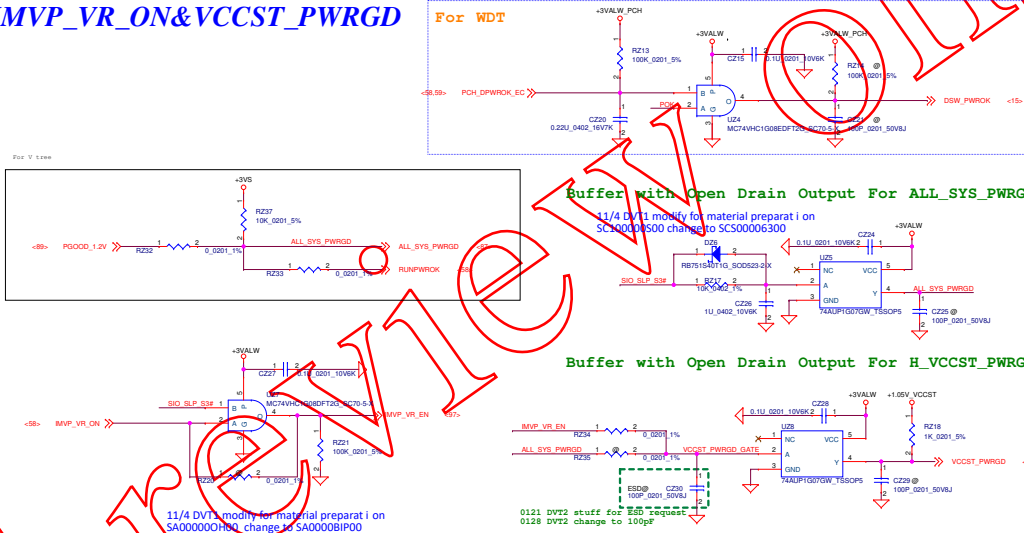


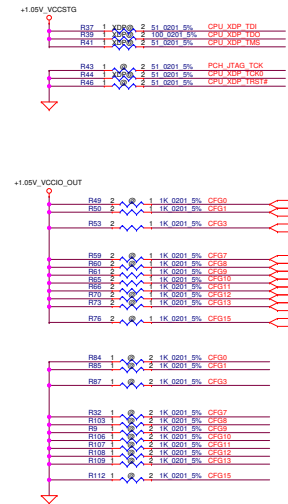
+1.2V

Sequence Logic



IMVP_VR_ON&VCCST_PWRGD

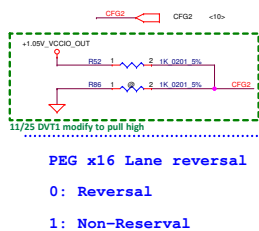




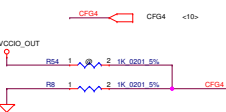
PEG x16 Lane reversal

0: Reversal

1: Non-Reversal

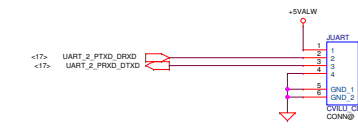
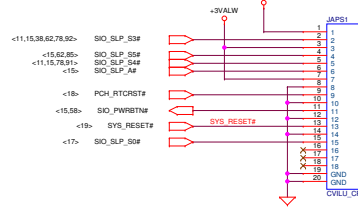


```
0 : enable
1 : disable
```

[illegible]

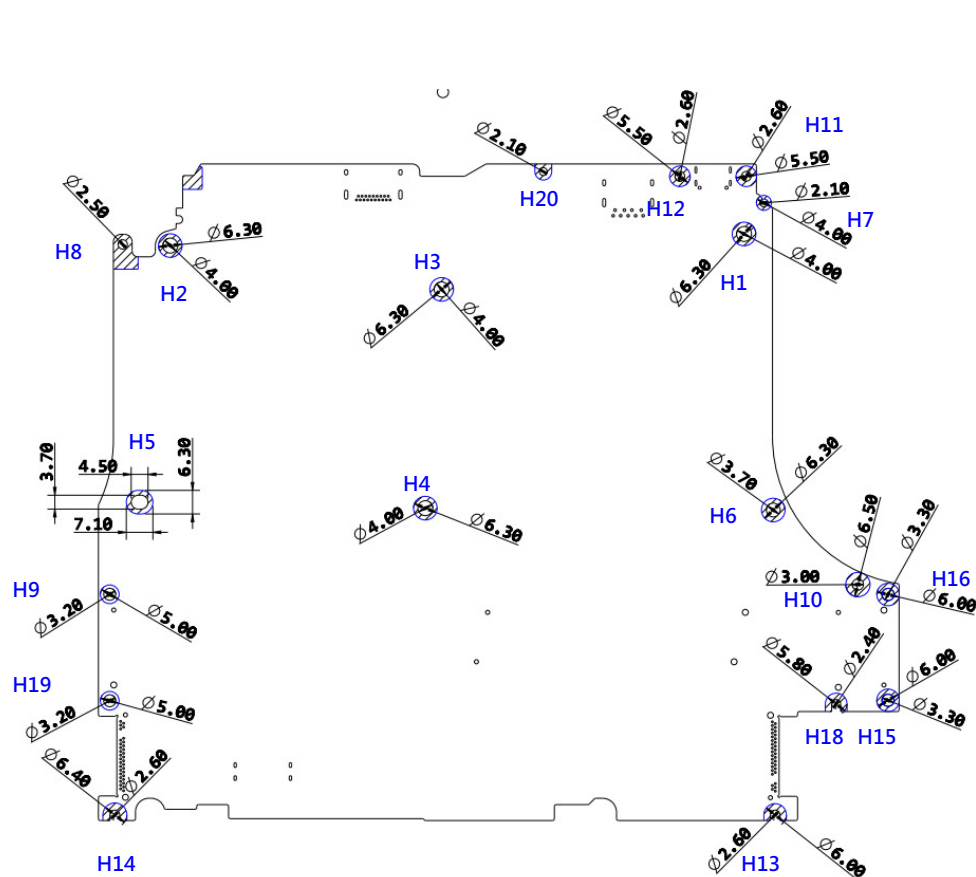
2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19

Pin connection diagram for UART module. The diagram shows two pins, `<17> UART_2_PTXD_DRXD` and `<17> UART_2_RXD_DTXD`, connected to a 5V pin and a GND pin on a connector. The connector also shows pins for `+5VSWV`, `UART` (pins 1-4), `GND 1`, `GND 2`, and `CPUVU CA CONN`.

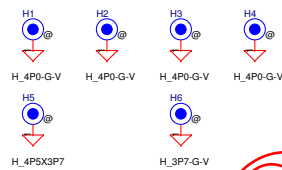
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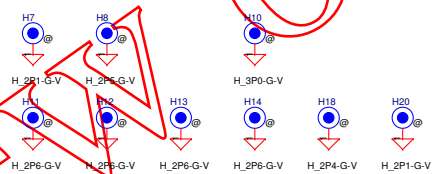
For DCA



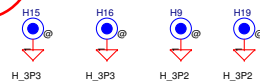
CPU & GPU



PTH



Stand-off

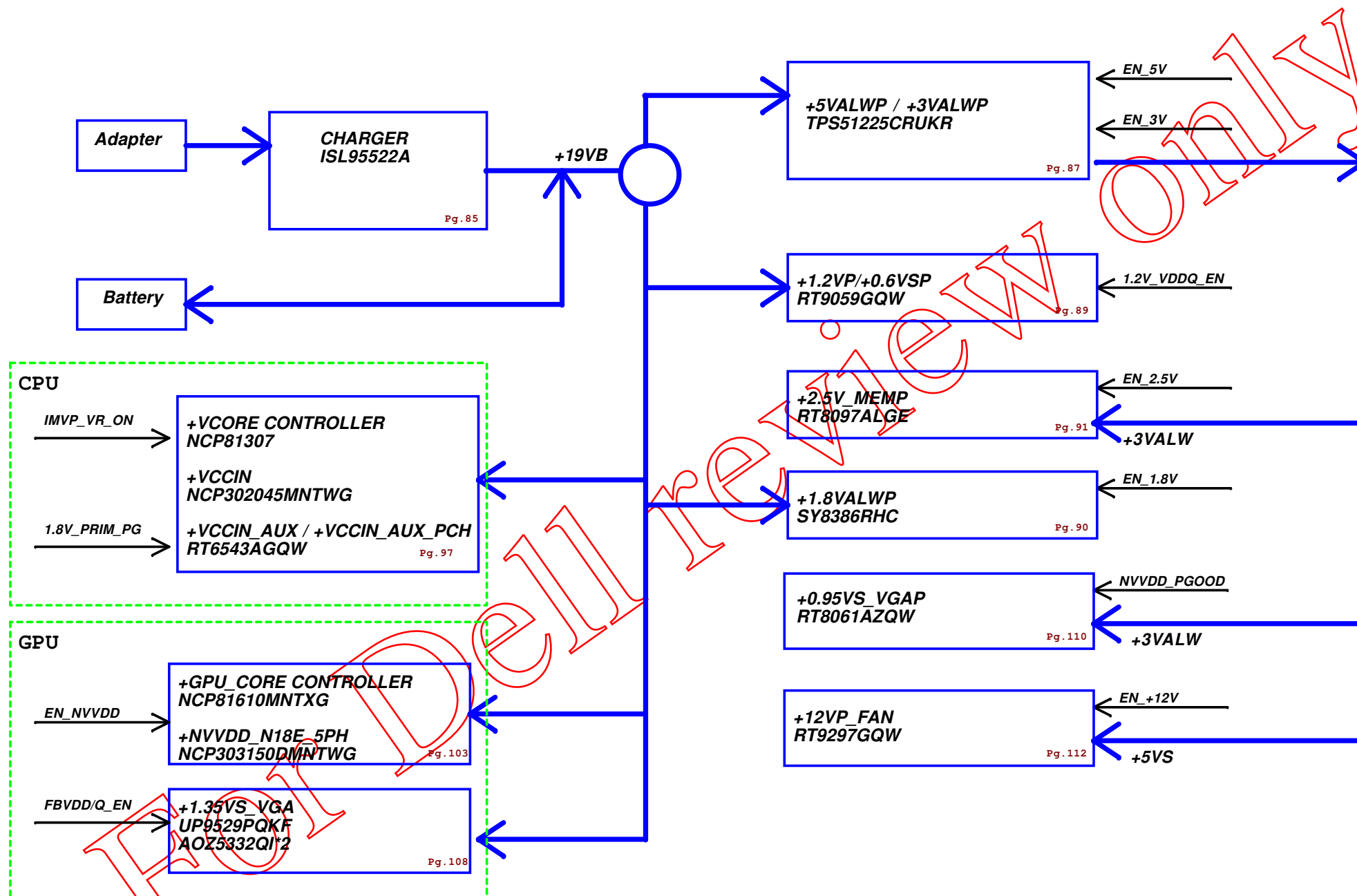


Fiducial Mark



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Power block

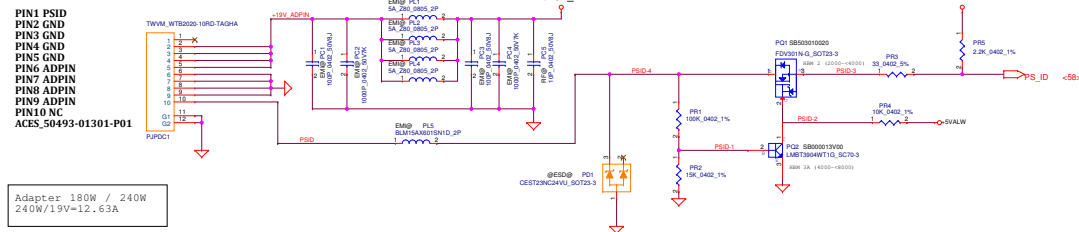


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Main Func = DCIN CONN

Adapter Connector

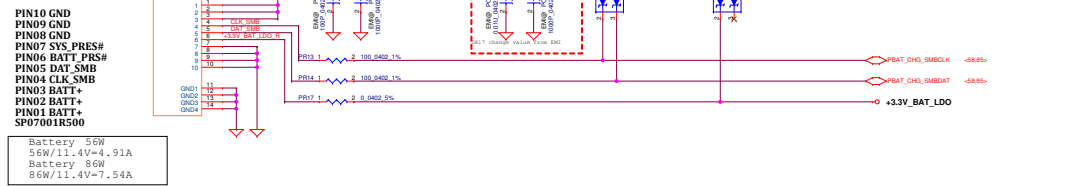
Adapter Bot Side



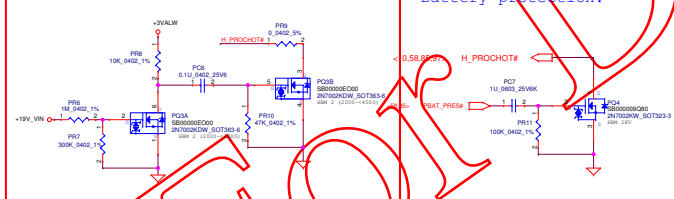
Main Func = BATT CONN

Battery Connector

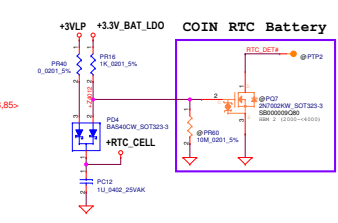
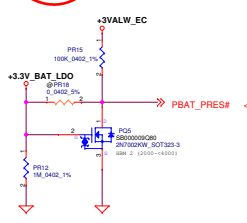
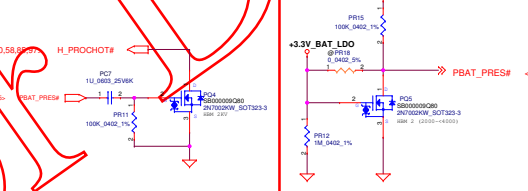
Battery Bot Side



Adapter protection:



Battery protection:



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Reserve

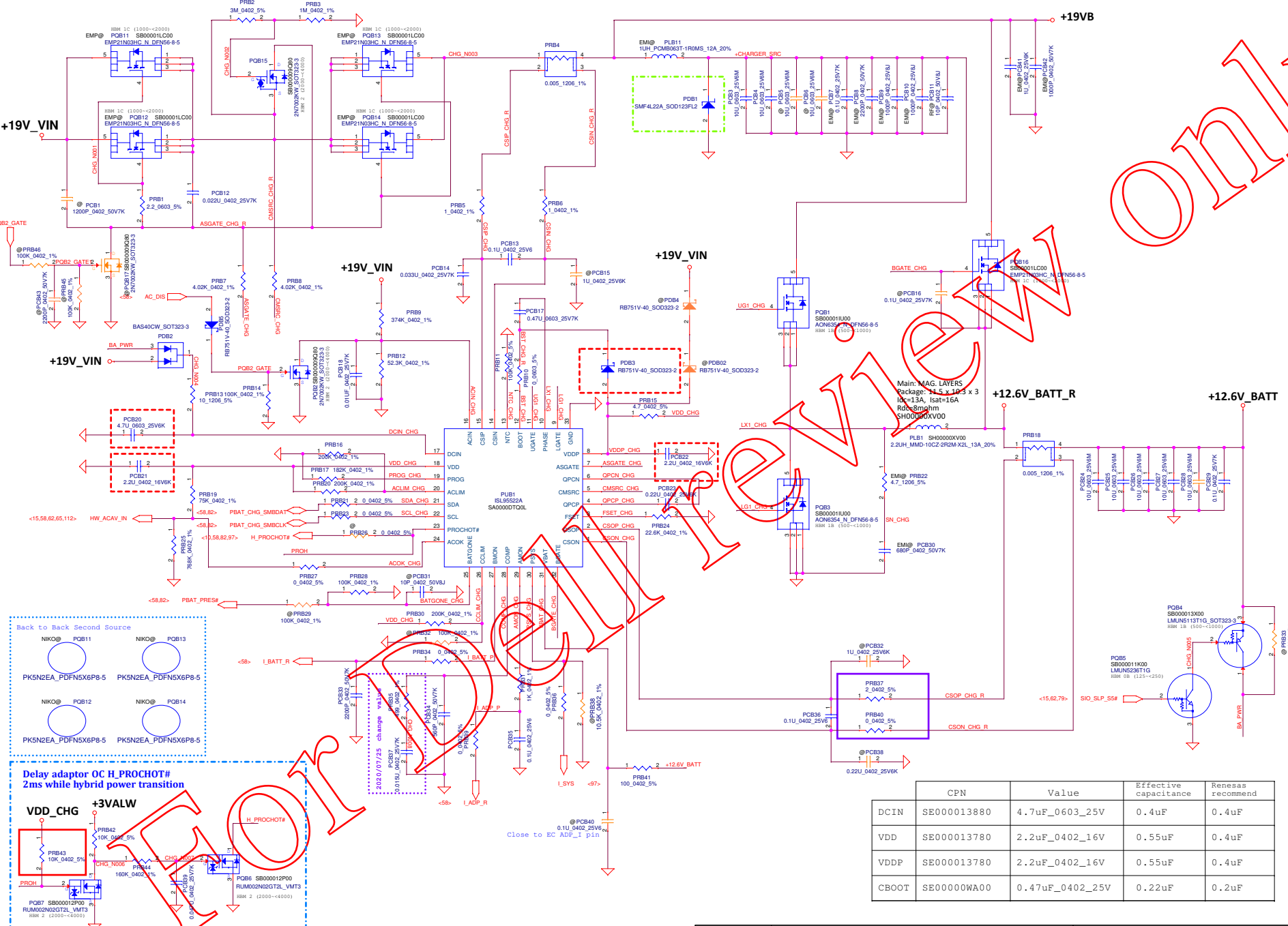
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Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	PWR-Reserve	
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Reserve

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Main Func = CHARGER



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Date: 2020.03.25.2021				

Main Func = 3.3VALWP / 5VALWP

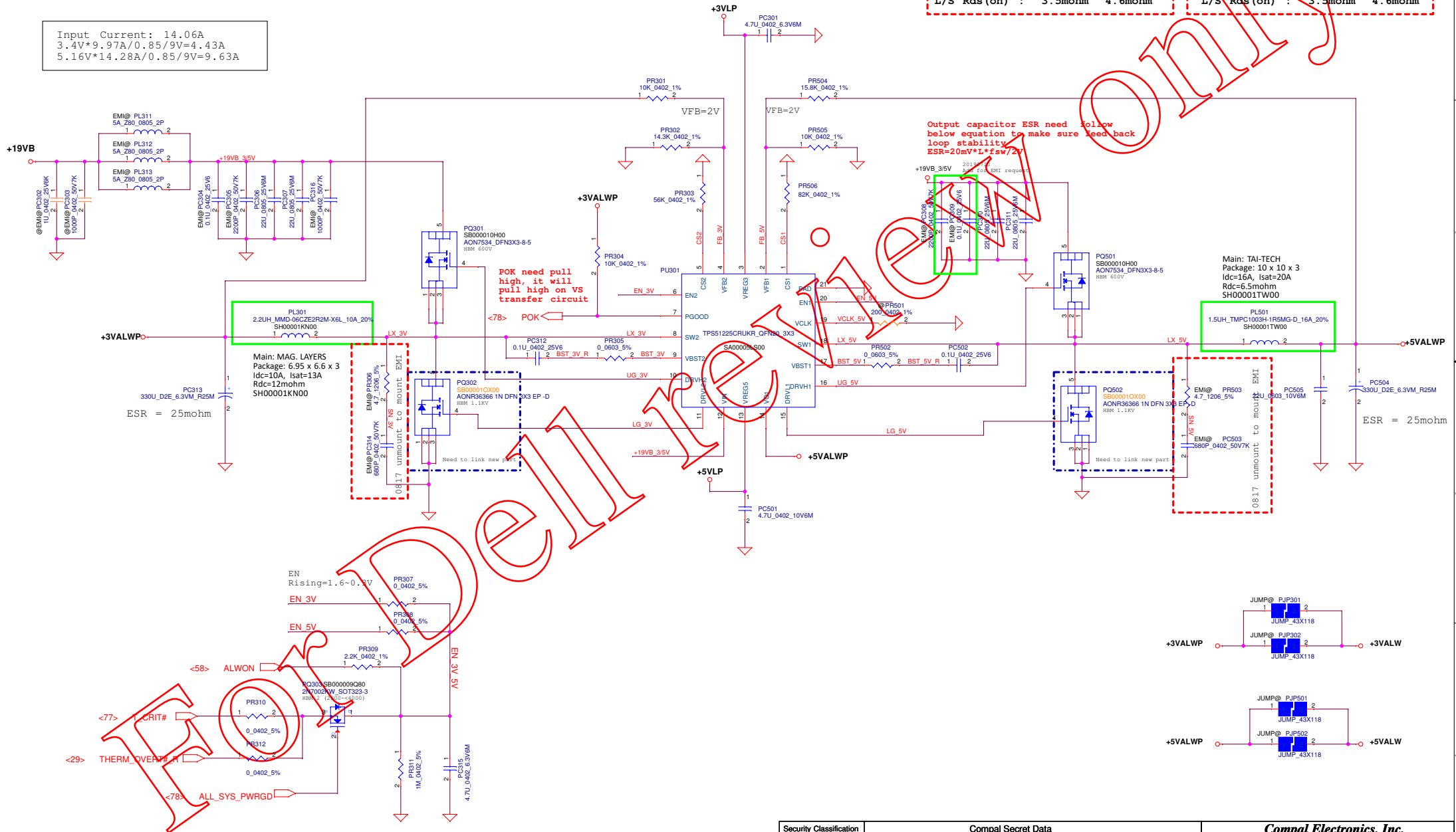
Input Current: 14.06A
 $3.4V \times 9.97A / 0.85 / 9V = 4.43A$
 $5.16V \times 14.28A / 0.85 / 9V = 9.63A$

```
3.3VALWP
Vout=3.4V
TDC 10A
Peak Current 11.5A
OCP current 13A
OVP=3.824V~3.994V(112.5%~117.5%)
UVP=1.869V~2.209V(55%~65%)
FSW=355kHz
```

MOS (VGS = 4.5V)		
	TYP	MAX
H/S Rds (on) :	6.7mohm	8.5mohm
L/S Rds (on) :	3.5mohm	4.6mohm

5VALWP
Vout= 5.16V
TDC 14.5A
Peak Current 17.7A
OCP current 21.24A
OVP=5.805V~6.063V(112.5%~117.5%)
UVP=2.838V~3.354V(55%~65%)
FSW=300kHz

MOS (VGS = 4.5V)		TYP	MAX
H/S	Rds (on)	6.7mohm	8.5mohm
L/S	Rds (on)	3.5mohm	4.6mohm



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				Issue Date 2020.03.25
				Rev 01
				1/4

Main Func = 1.2VP / 0.6VSP / 2.5V_MEMP

Input Current: 1.012A

$1.203V \times 5.92A / 0.85 / 9V = 0.93A$

$0.6V \times 1.05A / 0.85 / 9V = 0.082A$

Pin19 need pull separate from +1.2VP.
If you have +1.2V and +0.6V sequence question,
you can change from +1.2VP to +1.2VS.

+1.2VP
Vout= 1.203V
TDC 5.35A
Peak Current 7.64A
OCP current 10.12A
OVP=1.36V~1.44V (113%~120%)
UVP=0.72V~0.96V (60%~80%)
FSW= ~538 Hz

MOS (VGS = 4.5V)
H/S Rds(on) : 11mohm
L/S Rds(on) : 11mohm

+0.6VSP
Vout= 1.203V
TDC 1.0A
Peak Current 1.5A

+1.2VP
+1.2V_VDDQ_CPU
+0.6VSP
+0.6V_VDDQ_VTT

Main MAG, LAYERS
Package: 6.86 x 6.47 x 3
Idc=11.3A, Isat=11.3A
Rdc=6.2mohm
SH000000M00

Mode Level +0.6VSP VTTREF 1.2V
S5 L off off
S3 L off on
S0 H on on
Note: S3 - sleep ; S5 power off

$V_{out} = 0.75 \times (1 + PRM6 / PRM9)$
 $= 1.203V$

XMP1 Function
 $V_{out} = 0.75 \times (1 + PRM6 / (PRM9 // PRM14))$
 $= 1.354V$

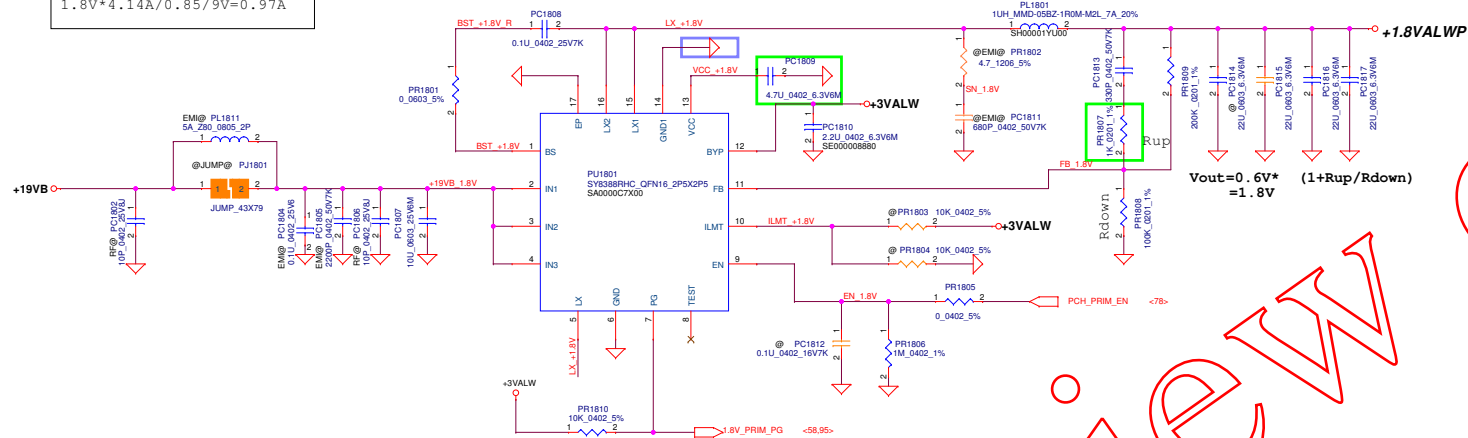
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				Size Document Number
				LA-K455P
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Main Func = 1.8VALWP

Input Current: 0.97A
 $1.8V \times 4.14A / 0.85 / 9V = 0.97A$

Main MAG. LAYERS
Package: 5.49 x 5.18 x 2
Idc=7A, Isat=13.7A
Rdc=18.9mohm
SH00001YU00

```
+1.8VALWP
TDC 5.35A
Peak Current 7.43A
Current limit 8A
OVP=2.106V~2.214V(117%~123%)
UVP=0.99V~1.17V(55%~65%)
FSW= 500K-Hz
```



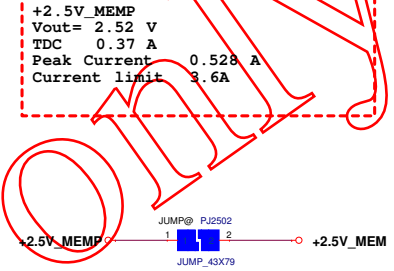
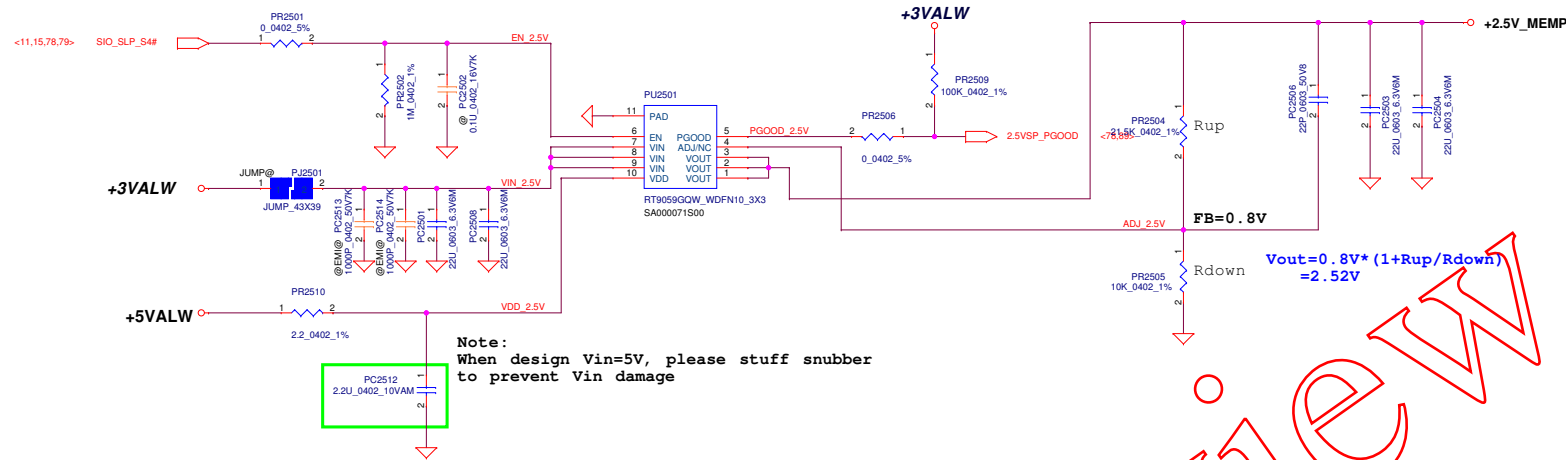
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Security Classification	Compal Secret Data		Title	
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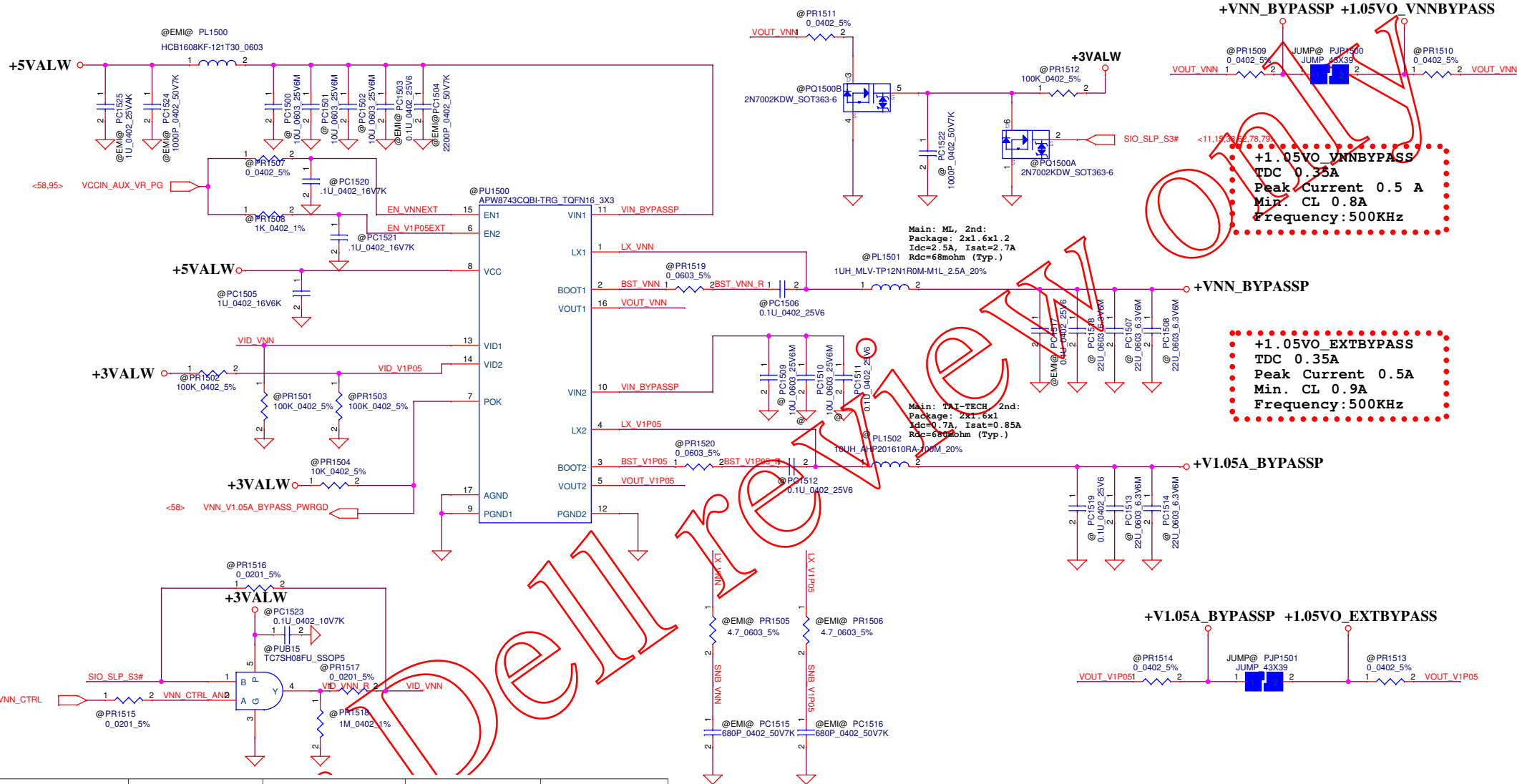
Main Func =2.5V_MEMP

Input Current: 0.366A

$2.52V \times 0.37A / 0.85 / 3V = 0.366A$



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+VNN_BYPASSP +1.05VO_VNNBYPASS



+1.05VO_VNNBYPASS
TDC 0.35A
Peak Current 0.5 A
Min. CL 0.8A
Frequency: 500KHz

+1.05VO_EXTBYPASS
TDC 0.35A
Peak Current 0.5A
Min. CL 0.9A
Frequency: 500KHz

+V1.05A_BYPASSP +1.05VO_EXTBYPASS



Part Number	VID=0(VNN)	VID=1(VNN)	VID=0(V1P05A)	VID=1(V1P05A)
APW8743CQBI(QBGI)	1.05V	0.78V	1.05V	0.96V
APW8743DQBI(QBGI)	0.78V	0.7V	1.05V	0.96V
APW8743EQBI(QBGI)	1.05V	0.7V	1.05V	0.96V

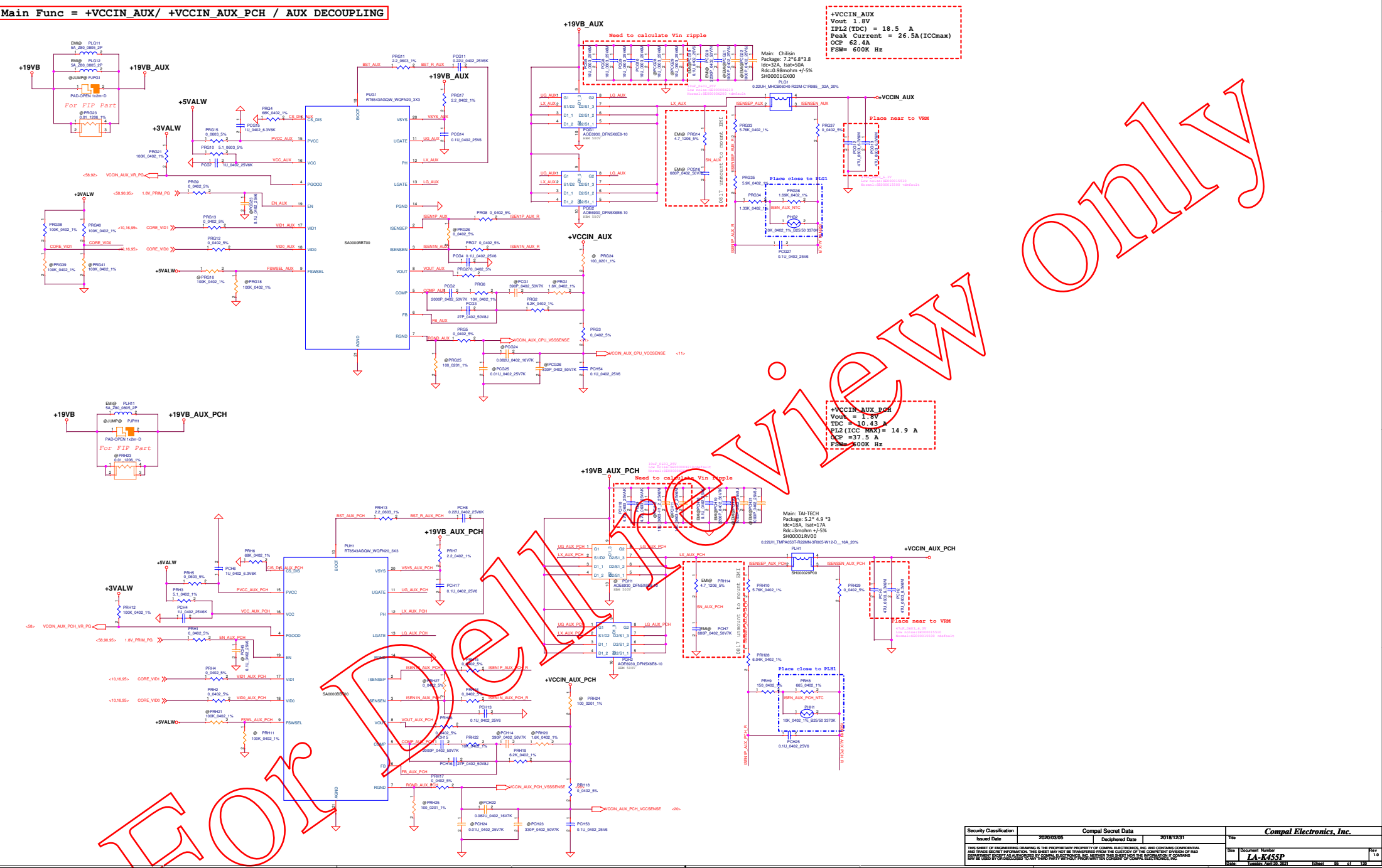
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Main Func = +VCCIN_AUX/ +VCCIN_AUX_PCH / AUX DECOUPLING

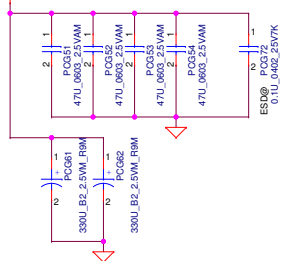


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+VCCIN_AUX Decoupling Cap

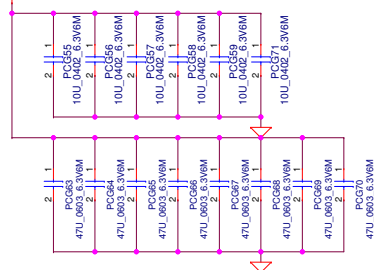
CPU Primary Side

+VCCIN_AUX



CPU Secondary side

+VCCIN_AUX



Follow Intel PDG Rev0.5 excel
+VCCIN_AUX Output CAP :

CPU Primary Side:
330uF_B2 *2pcs
47uF_0603 *4 pcs

CPU Secondary side:
10uF_0402 *6pcs
47uF_0603 *8pcs

For FIVR solution
15pF_0201 *6
12pF_0402 *6
on EE side (20200214)

+VCCIN_AUX_PCH Decoupling Cap

CPU Primary side

+VCCIN_AUX_PCH



Follow Intel PDG Rev0.5 excel
+VCCIN_AUX_PCH Output CAP :

CPU Primary Side:
47uF_0603 *5 pcs (Near PCH)
10uF_0402 *4 pcs (Near PCH)

on EE side (20200214)

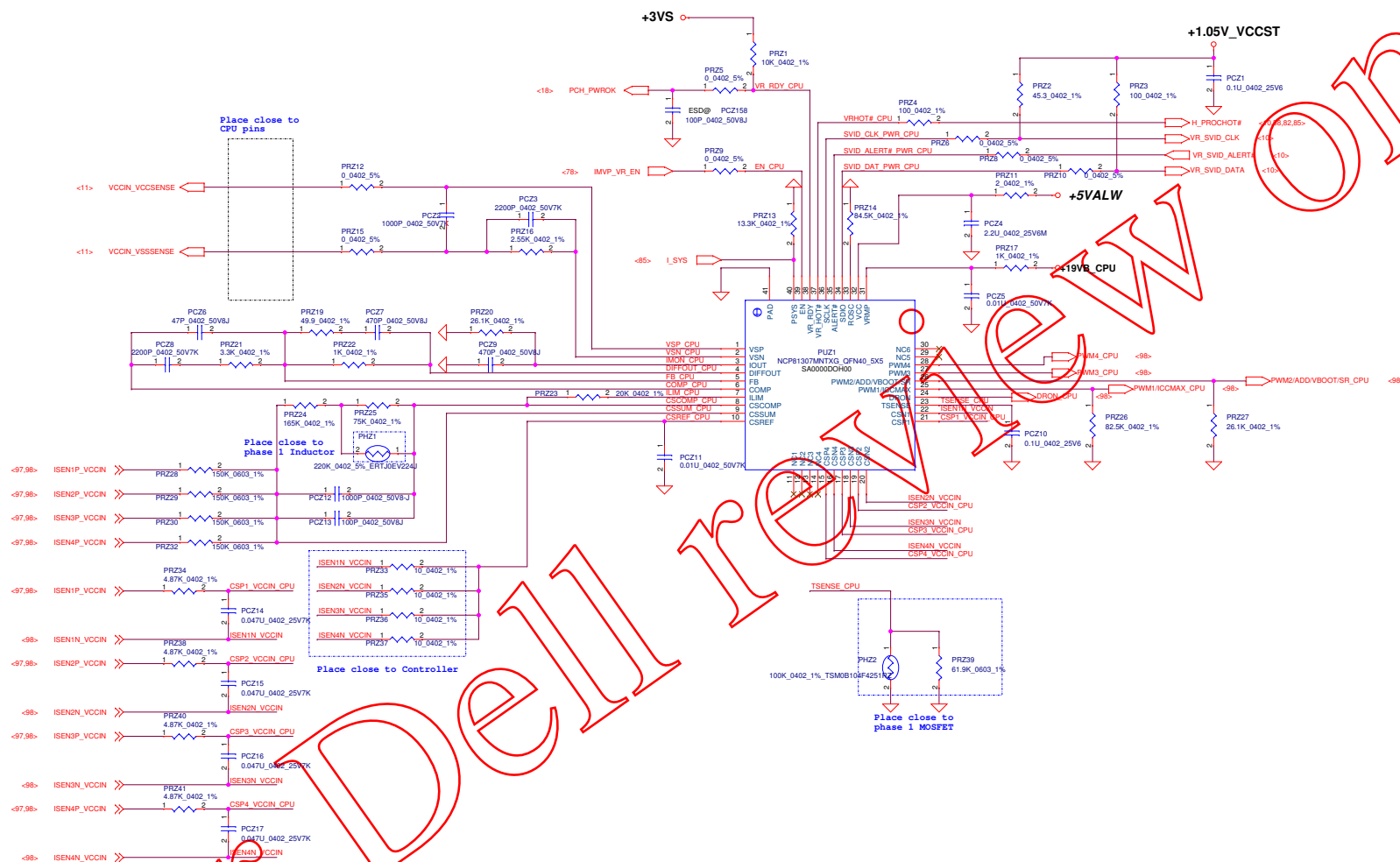
reserve 47uF_0603 *2 pcs on PWR side (20200406)

For Dell review

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Issued Date	2020/03/05	Deciphered Date	2018/12/31	
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				Document Number
				LA-K455P
				Rev
				1.0
Date: Tuesday, April 20, 2021		Sheet 96 of 120		

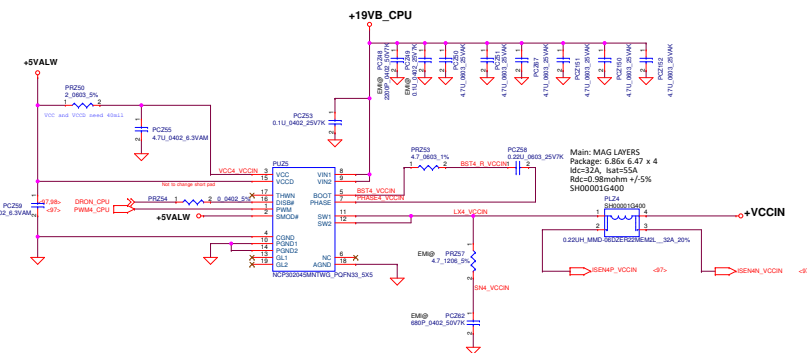
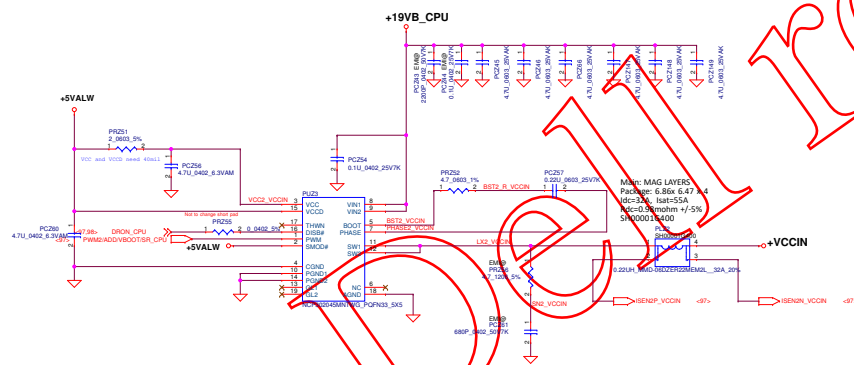
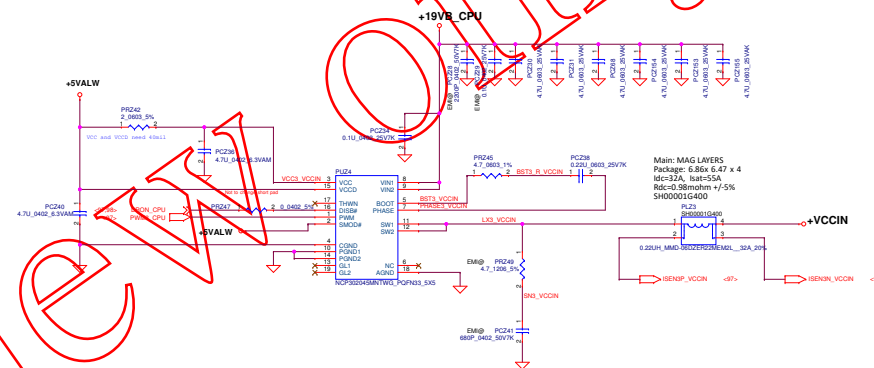
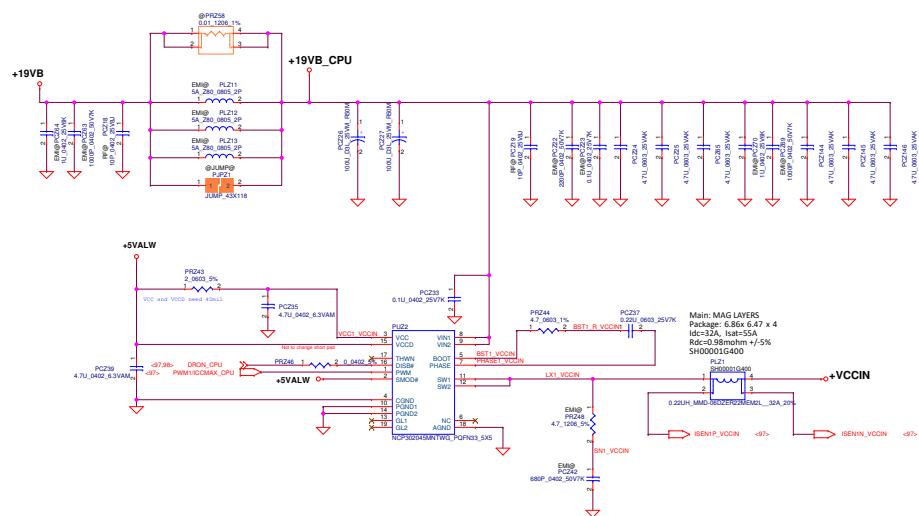
Main Func = CPU

+VCCIN
Vout = 2.05V
IPL2 = 61A
Peak Current = 105A (ICCMAX)
DC Load line: NA
AC Load line: NA
Current limit = 137A (OCP)
FSW = 600K Hz



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```
+VCCIN
Vout(max) = 2.05V
IPL2 = 61A
Peak Current = 105A(ICCmax)
DC Load line:NA
AC Load line:NA
Current limit = A(OCP)
FSW = 600K Hz
```



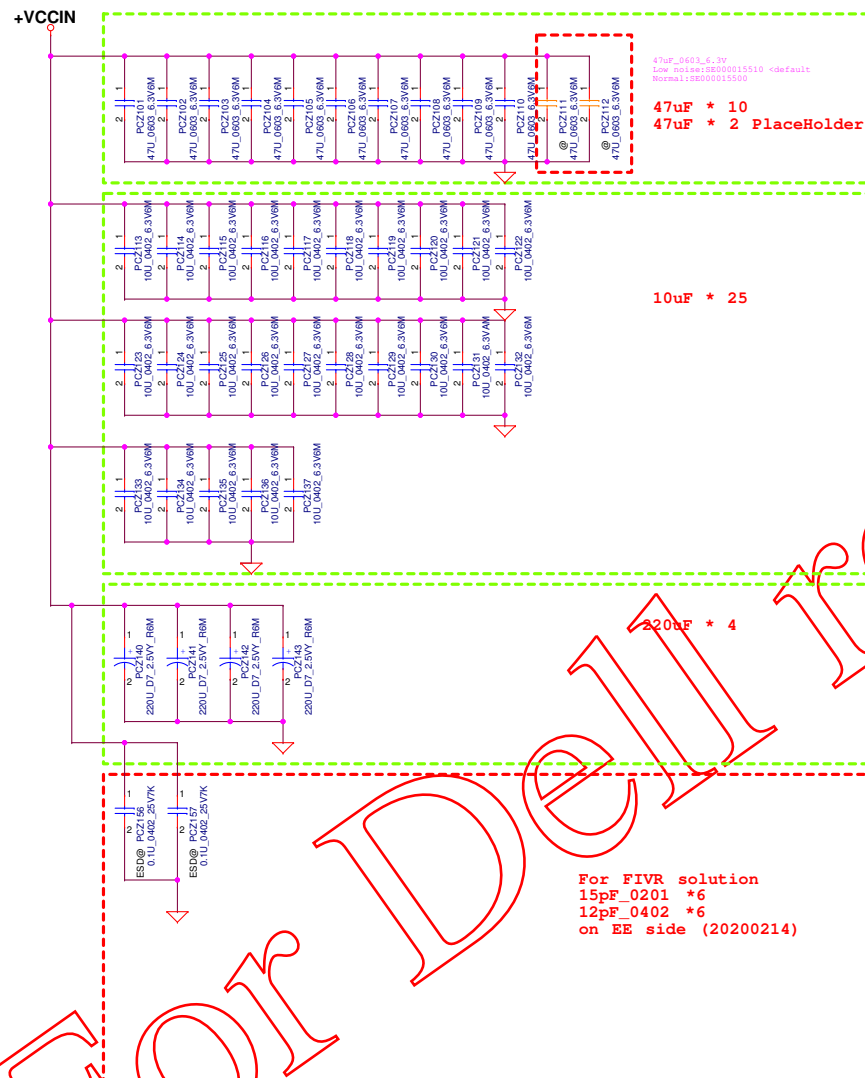
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Date	Issued	2020	3/25	1/4	

Main Func = +VCCIN DECOUPLING



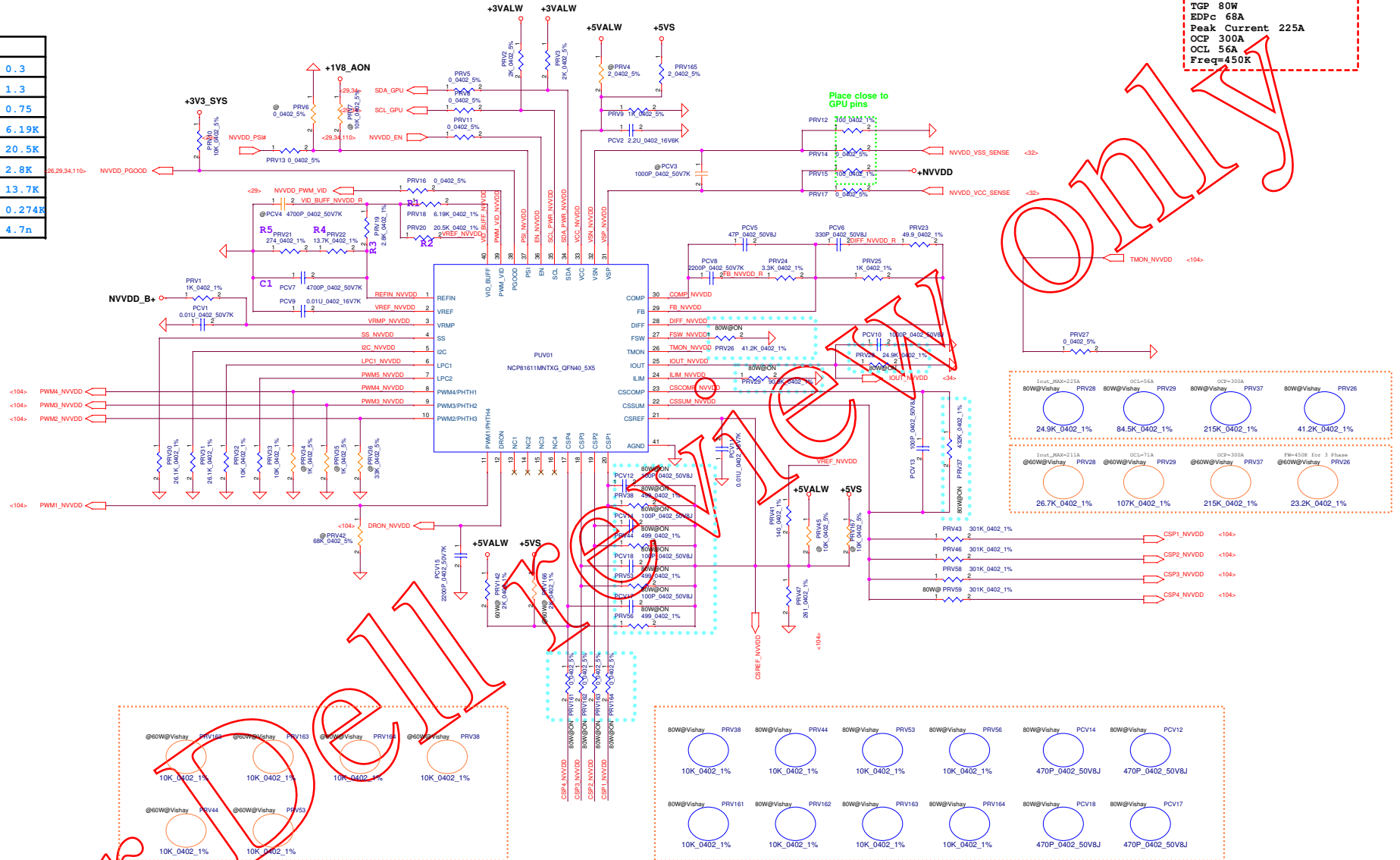
Follow Intel PDG Rev0.5 excel
+VCCIN Output CAP :
47uF_0603 *10 pcs + reserved *2pcs
10uF_0402 *25 pcs
220uF_D7 *4pcs

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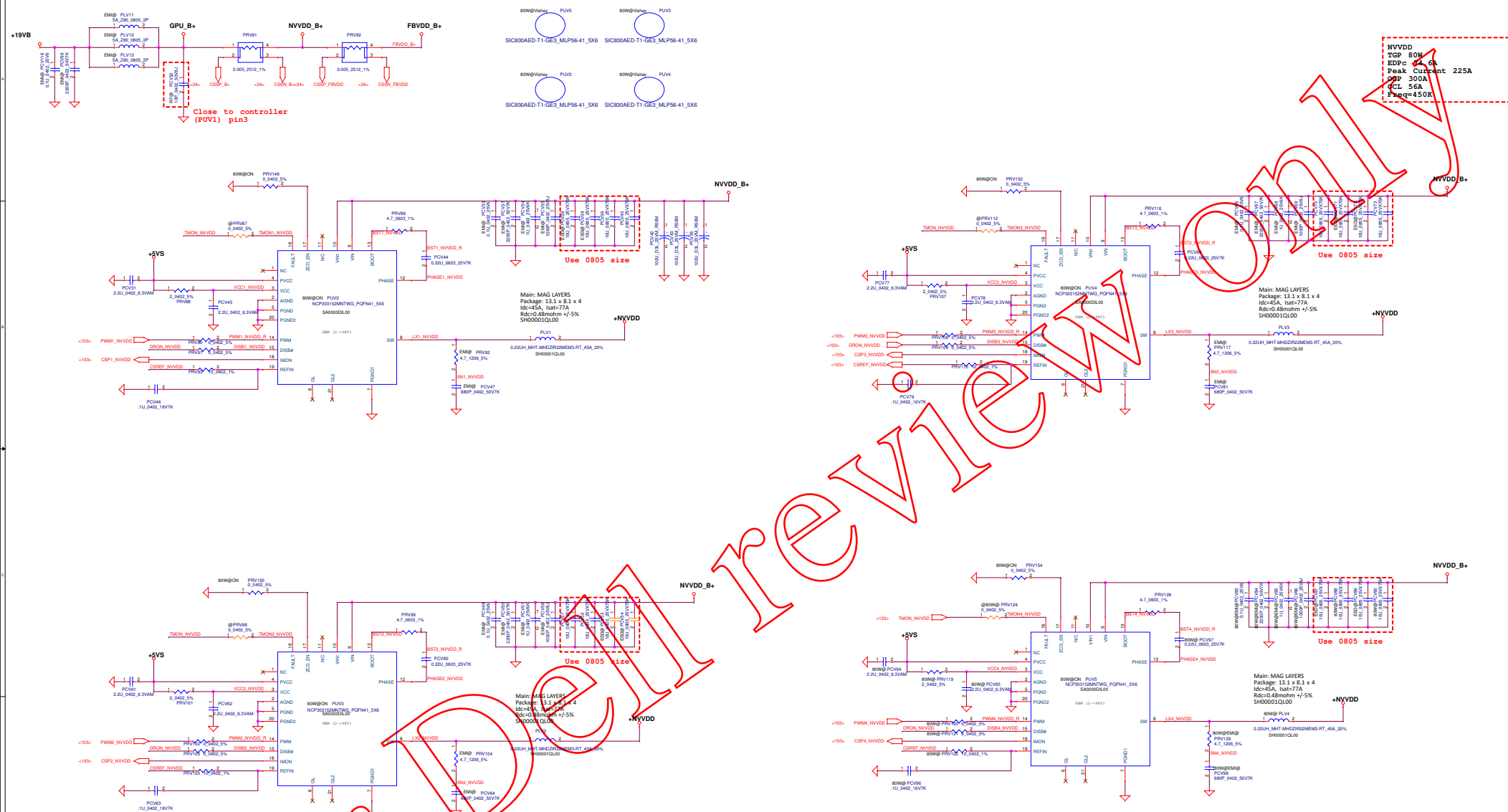
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				Date	Issued	2020.03.25	100	21	120

Main Func = VGA CORE

Config	
Vmin	0.3
Vmax	1.3
Vboot	0.75
R1	6.19K
R2	20.5K
R3	2.8K
R4	13.7K
R5	0.274K
C	4.7n



Security Classification	Compal Secret Data	Date	Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date	2020/04/19
Title			PWR VGA NCP8161MNTXG
Rev			1.0
Date			Tuesday, April 20, 2021
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Issued Date	2000/03/05	Deciphered Date	2020/04/19	Title
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Date: Tuesday, April 20, 2021				Sheet	105 of 120	

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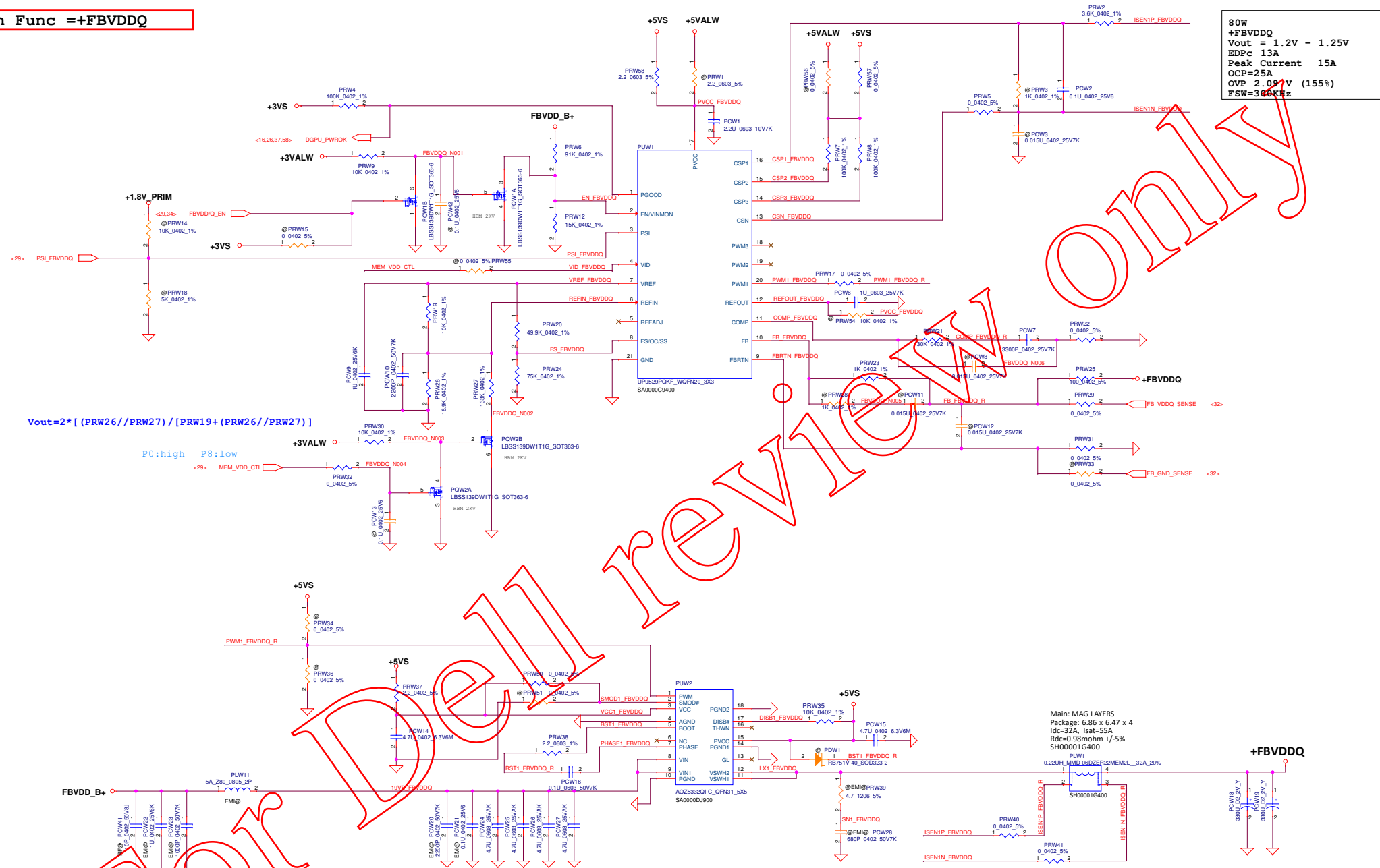
Main Func = VGA CORE DECOUPLING

+NVVDD
330uF X 4
22uF_0805 X 15
10uF_0603 X 34
1uF_0402 X 13

Place under GPU

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/04/18	Declassified Date	2020/04/18	Title	PWR_VGA_NCP30315
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				Doc No.	LA-K455P
				Date	Issued: 2018.04.18

Main Func = +FBVDDQ



BOM config	GPU type	VRAM memory	VRAM vender	RVL	PRW30	PRW31
	GN20E			1.25V	16.9K	
				1.2V	16.9K	133K

Security Classification	Compal Secret Data			Title				
Issued Date	2020/03/05	Deciphered Date	2020/04/19	PWR +1.35VRAM				
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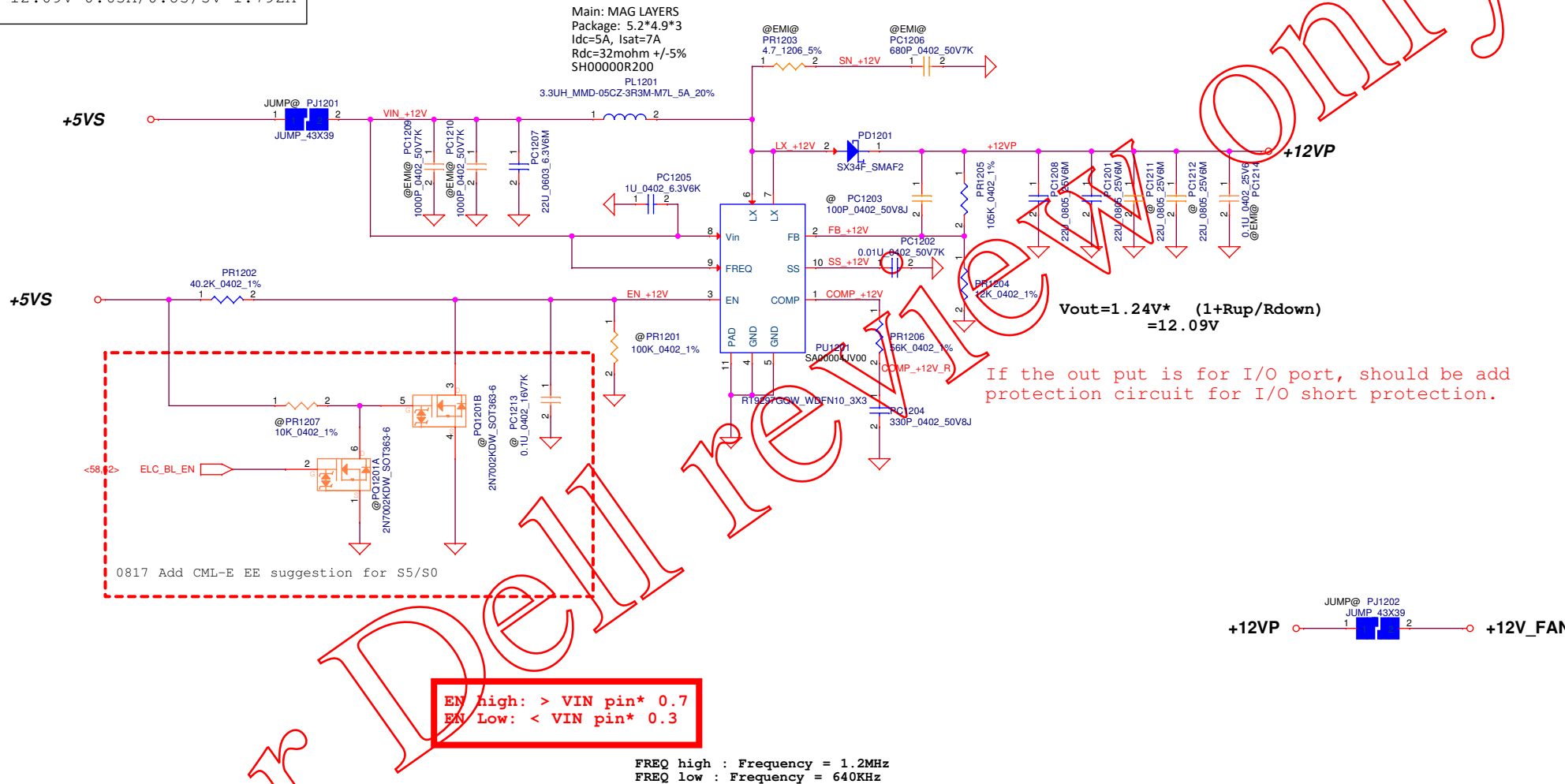
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Main Func =+12VP_FAN

Add a switch circuit to turn off the +12V_VIN if need.

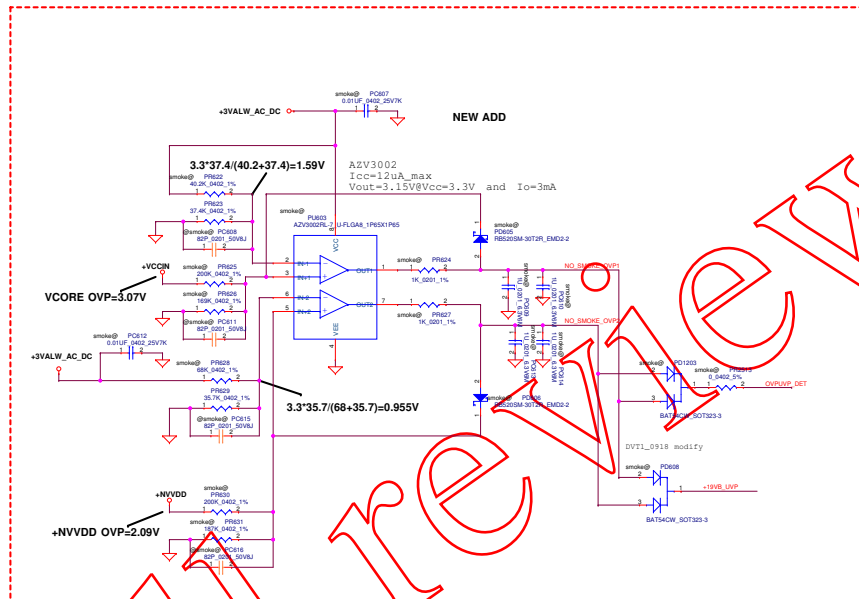
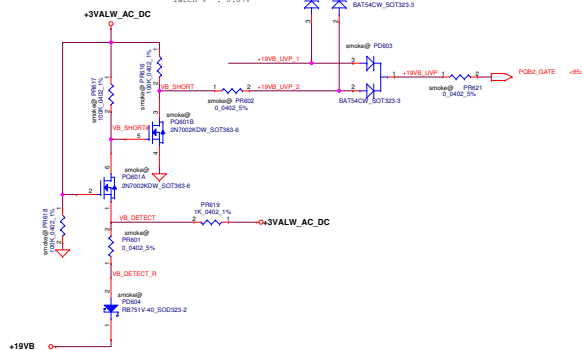
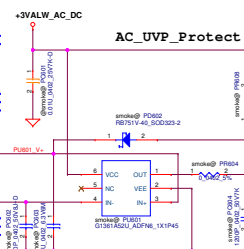
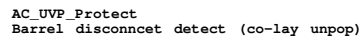
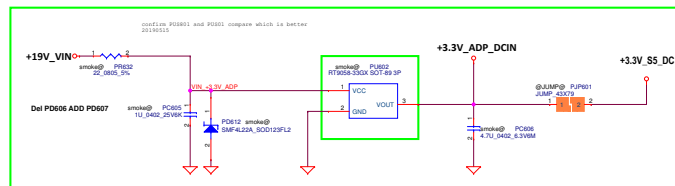
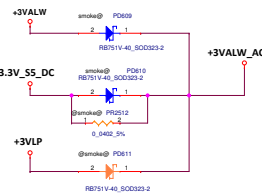
Input Current: 1.792A
 $12.09V \times 0.63A / 0.85 / 5V = 1.792A$

+12VP
Vout = 12.09 V
TDC 0.63A
Peak Current 0.9A
Current limit 3A
FSW=1.24MHz



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Issued Date	2020/03/05	Deciphered Date	2018/12/31	Title	PWR +12VP FAN		
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Main Func = Smokeless UVP



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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	51, 52	PWR_Dual adapter1 (ISL95338) PWR_Dual adapter2 (ISL95338)	7/18	PWR	1. Removal adapter, ACOK doesn't pull low	1. PDS01, PDS02 change from SCS00003800 to SCS00000200.	X01
2	50	DC/BATT Conn/OTP/RTC	7/18	PWR	1. Because M/B mark DCIN1/DCIN2 is different with connector location, we exchange the DC-IN location.	1. PJPDC1 change to PJPDC2. 1. PJPDC2 change to PJPDC1.	X01
3	51, 52	PWR_Dual adapter1 (ISL95338) PWR_Dual adapter2 (ISL95338)	7/18	PWR	1. For reducing S5 power consumption.	1. Add B2B PMOS bypass circuit	X01
4	51, 52	PWR_Dual adapter1 (ISL95338) PWR_Dual adapter2 (ISL95338)	7/18	EMI	1. Because EMI test fail, request us to change 1.5uH ISN choke.	1. Change PQS01, PQS06, PQS10, PQS11 from SH000001E00 to SH000016700.	X01
5	51, 52 53, 54 55, 56 57	PWR_Dual adapter1 (ISL95338) PWR_Dual adapter2 (ISL95338) PWR_+1VALWP PWR_+1.2VP/+0.6VSP PWR_CHARGER PWR_+VCCIOP	7/18	PWR	1. Because materials lackage, sales request us to downsize MLCC.	1. Change PCS20, PCS21, PCS23, PCS49, PCS50, PCS52, PC1801, PC302, PC318, PC319 size from 0603 to 0402. 2. Change PC104, PC202, PC203, PC205, PC206, PC761, PC766, PC775, PCF03 size from 0805 to 0603. 3. Change PC212, PCF15 size from 0201 to 0402.	X01
6	59, 60	PWR_VCORE_ISL95829C PWR_+VCC_CORE	7/18	PWR	1. Modify CPU IC 's IMON, comp, loadline for meet Intel spec.	1. Change the PRZ39 from 80.6kOhm to 76.8kOhm 2. Change the PRZ36 from 4.42kOhm to 2.61kOhm 3. Change the PRZ29 from 2.61kOhm to 4.42kOhm 4. Change the PRZ33 from 604 Ohm to 523 Ohm 5. Change the PCZ09 from 680pF to 1500pF 6. Change the PCZ31 from 680pF to 1500pF 7. Change the PRZ43 from 3.65kOhm to 1.27kOhm 8. Change the PCZ30 from 2200pF to 8200pF 9. Change the PRZ38 from 499 Ohm to 1kOhm 10. Change the PCZ25 from 1200pF to 100pF 11. Change the PRZ17 from 165kOhm to 150kOhm 12. Change the PCZ23 from 0.22uF to 0.022uF 13. Change the PRI18, PRI33, PRI59, PRI74, PRI99, PRI114 from 3.65kOhm to 7.15kOhm.	X01
7	51, 52	PWR_Dual adapter1 (ISL95338) PWR_Dual adapter2 (ISL95338)	7/23	PWR	1. For independent net name to control PMOS and FWEN switch.	1. Add net name OFF_PMOS_1, OFF_FWEN_1 2. Add net name OFF_PMOS_2, OFF_FWEN_2	X01
8	50	DC/BATT Conn/OTP/RTC	7/23	PWR	1. ISL95338 ACOK signal change from IC PWRGD to DCIN connector divided voltage.	1. Add PR36, PR38 1M ohm 2. Add PR35, PR37 205K ohm 3. 19V_VIN divided voltage 3.3V to EC as ACOK signal.	X01
9	60, 61, 62	PWR_VCC_CORE	7/24	PWR	1. Modify CPU IC 's IMON, comp, loadline for meet Intel spec.	1. Change the PRI202, PRI216, PRI228 from 1.74kOhm to 30.1kOhm.	X01
10	51, 52	PWR_Dual adapter1 (ISL95338) PWR_Dual adapter2 (ISL95338)	7/24	PWR	1. Avoid for adapter VIN spike.	1. Add PDS03/PDS04 SMF4L22A.	X01

Security Classification		Compal Secret Data		Title	
Issued Date	2020/03/05	Deciphered Date	2018/12/31	PWR PIR	
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